

Napredni mikroprocesorski sistemi

Uvod

Proizvodnja procesora

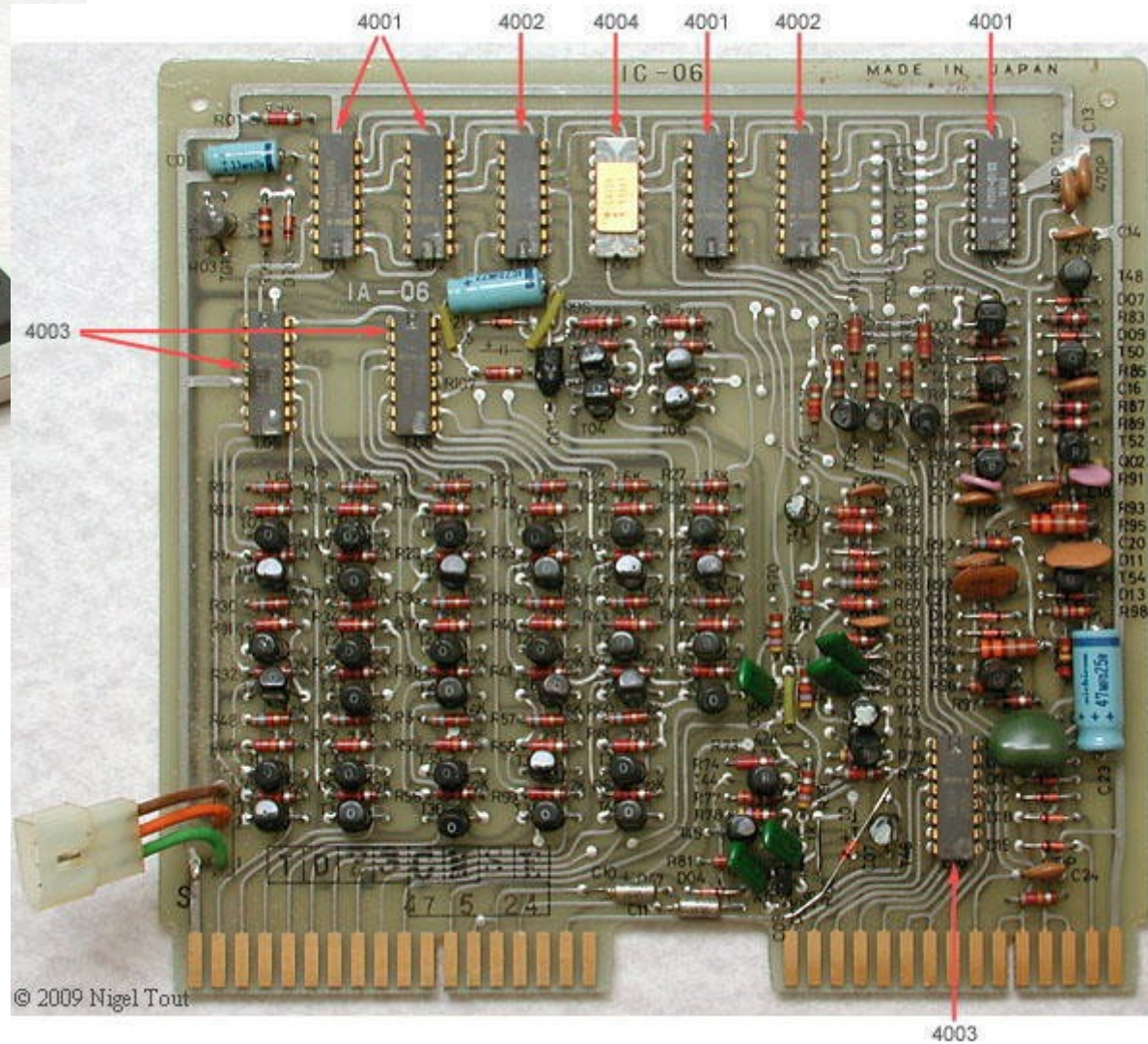


<https://www.intel.co.uk/content/www/uk/en/history/museum-story-of-intel-4004.html>

Proizvodnja procesora

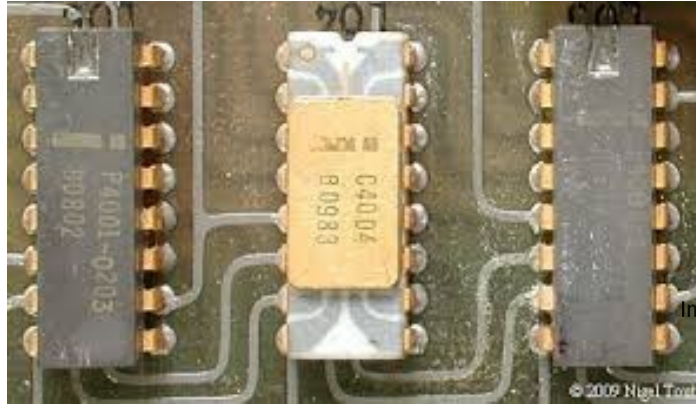


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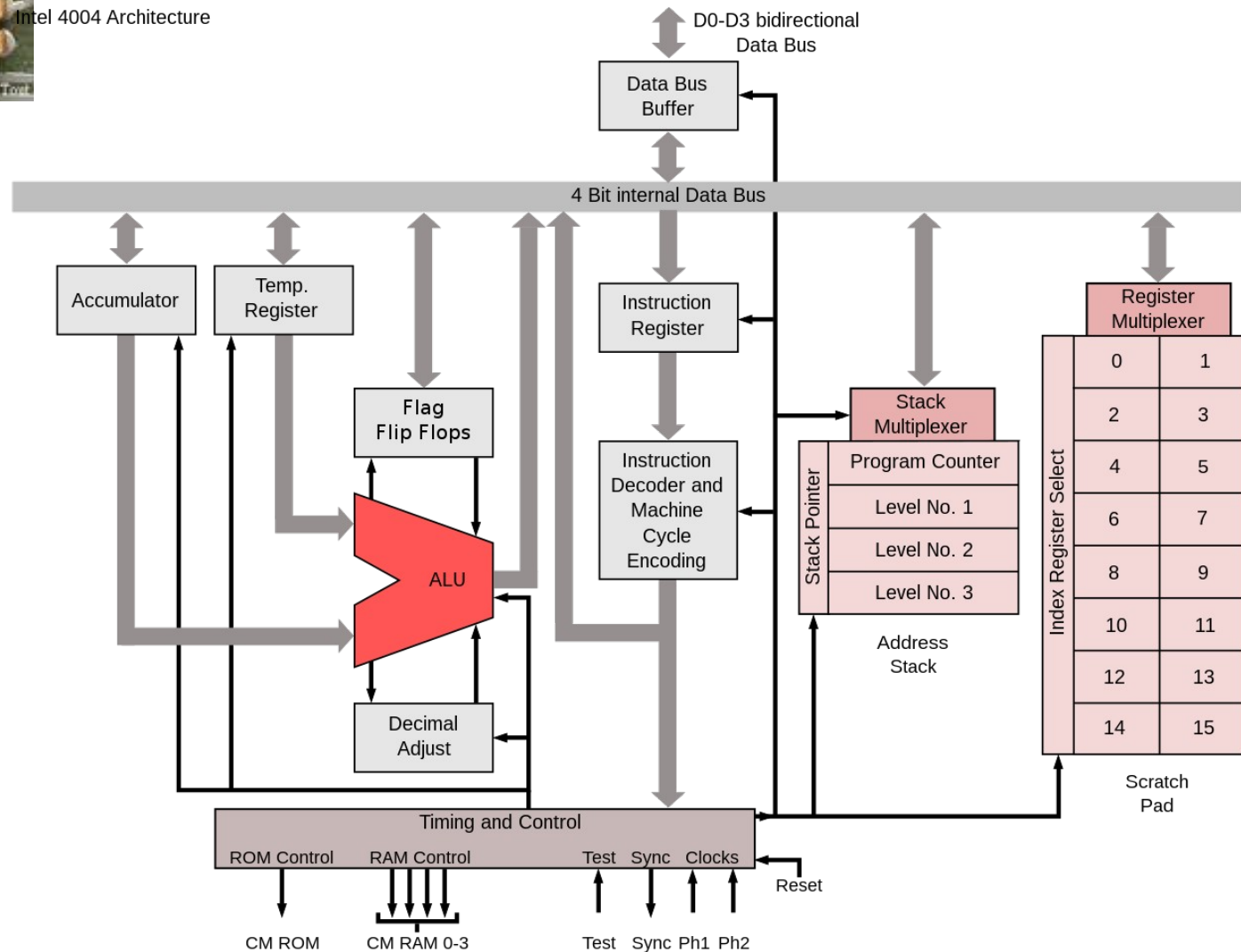


© 2009 Nigel Tout

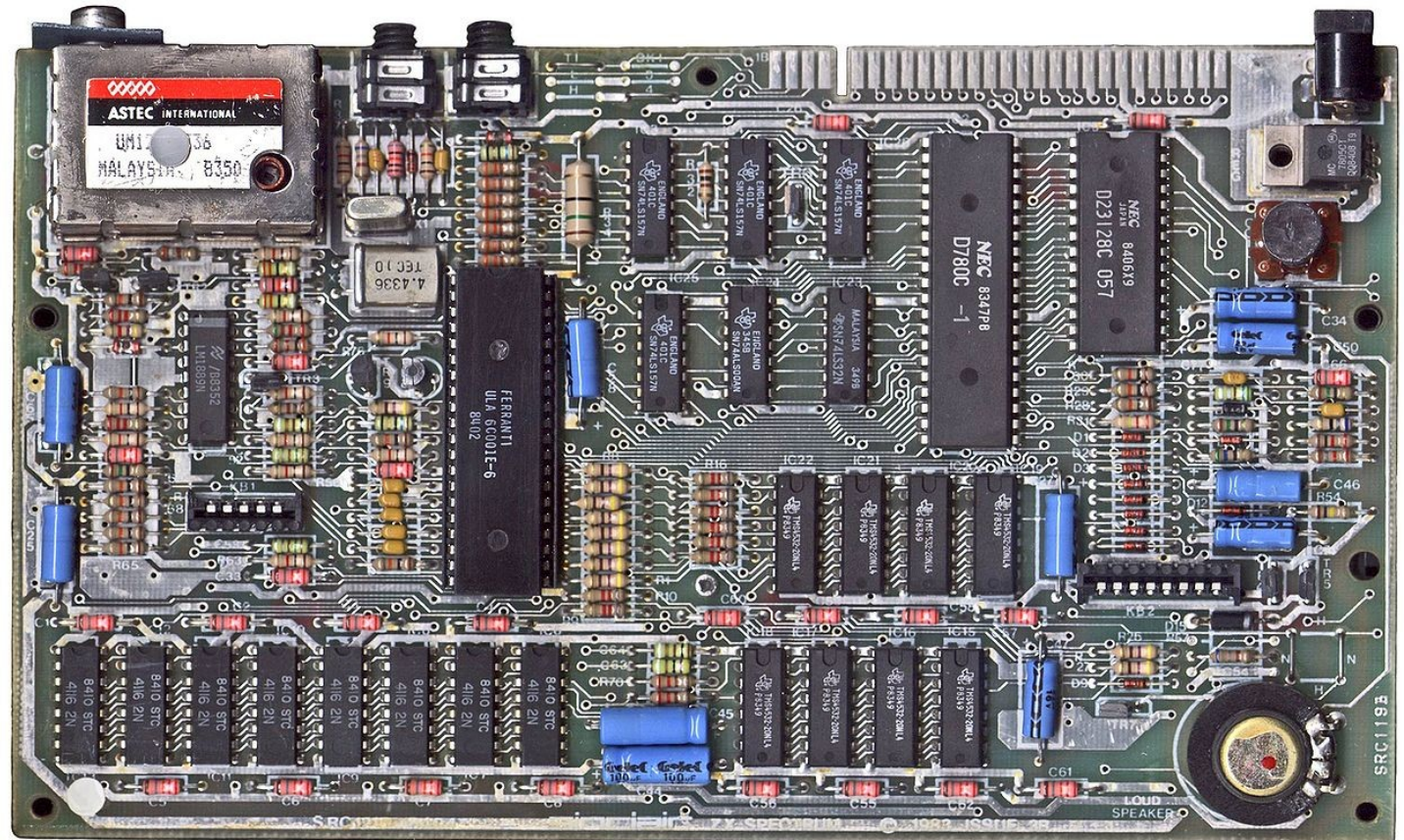
Proizvodnja procesora



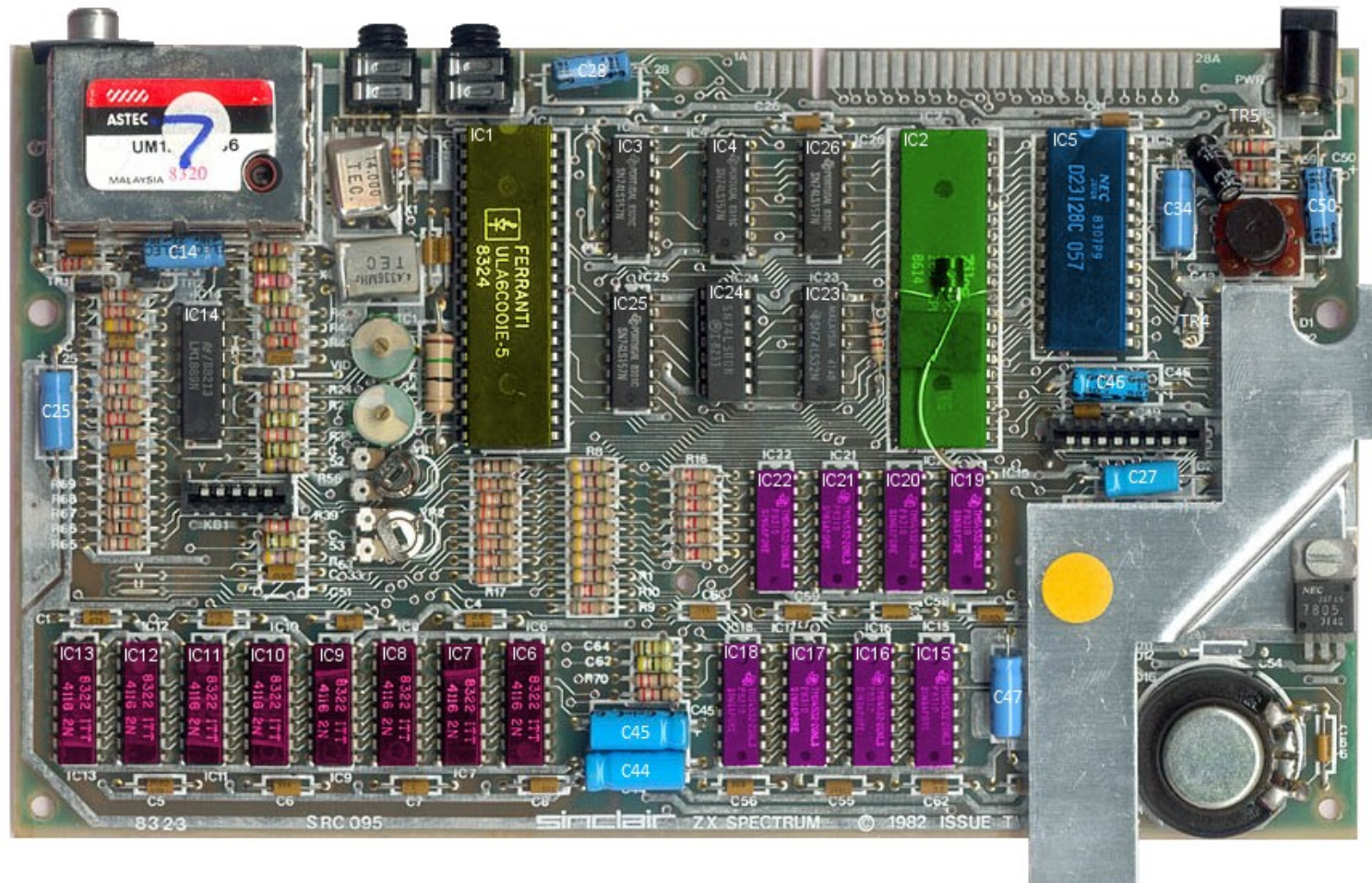
Intel 4004 Architecture



Proizvodnja procesora



Proizvodnja procesora



Integrated Circuits

Most of the chips are soldered to the board, with the exception of the ROM and the ULA

- IC1 - ULA
- IC2 - Zilog Z80A Processor
- IC3, IC4, IC23 to IC26 - Decoder / Multiplexor chips
- IC14 - LM1889N TV Video Modulator
- IC5 - HN613128P 16K ROM chip containing BASIC interpreter (&0000 - &3FFF)
- IC6 to IC13 - 4116 RAM chips for the lower 16K of memory (&4000 - &7FFF)
- IC15 to IC22 - 4532 RAM chips for the upper 32K of memory (&8000 - &FFFF)

90' Era personalnih računara



Intel pentium 1,2,3,4



(a) 1970s Processors

	4004	8008	8080	8086	8088
Introduced	1971	1972	1974	1978	1979
Clock speeds	108 kHz	108 kHz	2 MHz	5 MHz, 8 MHz, 10 MHz	5 MHz, 8 MHz
Bus width	4 bits	8 bits	8 bits	16 bits	8 bits
Number of transistors	2300	3500	6000	29,000	29,000
Feature size (μm)	10		6	3	6
Addressable memory	640 Bytes	16 kB	64 kB	1 MB	1 MB

(b) 1980s Processors

	80286	386TM DX	386TM SX	486TM DX CPU
Introduced	1982	1985	1988	1989
Clock speeds	6 MHz–12.5 MHz	16 MHz–33 MHz	16 MHz–33 MHz	25 MHz–50 MHz
Bus width	16 bits	32 bits	16 bits	32 bits
Number of transistors	134,000	275,000	275,000	1.2 million
Feature size (μm)	1.5	1	1	0.8–1
Addressable memory	16 MB	4 GB	16 MB	4 GB
Virtual memory	1 GB	64 TB	64 TB	64 TB
Cache	—	—	—	8 kB

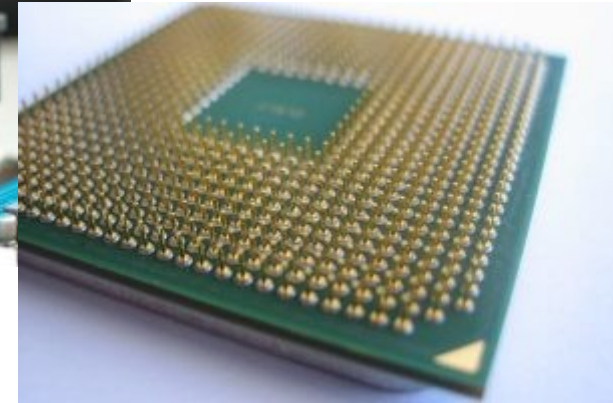
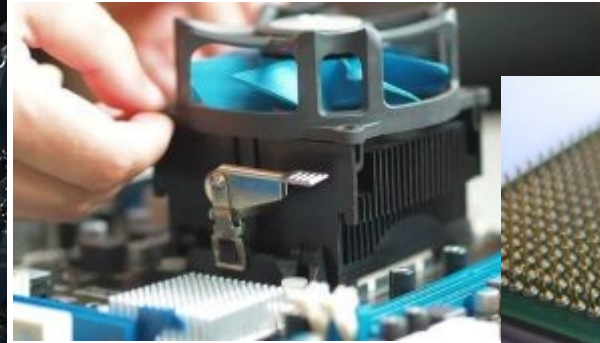
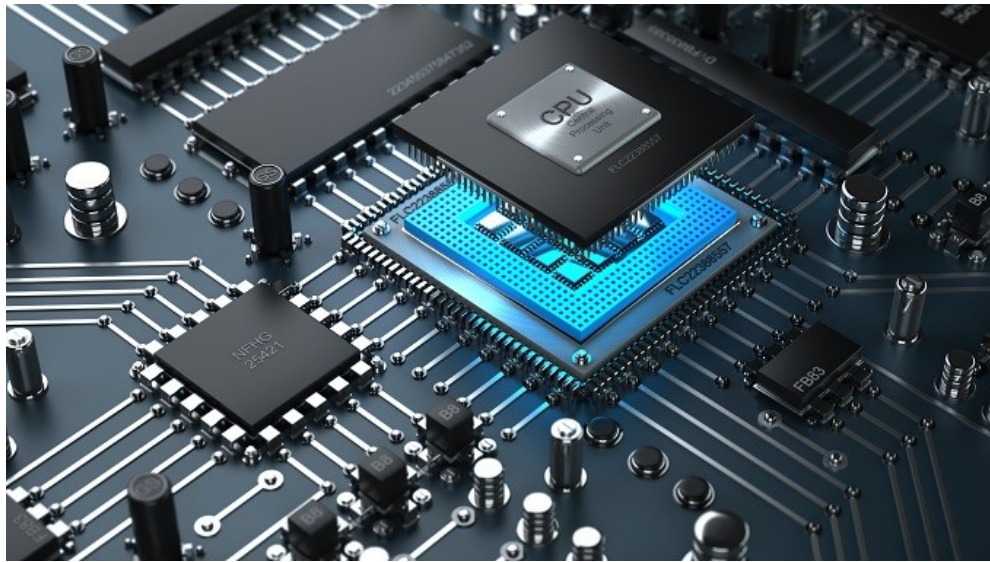
(c) 1990s Processors

	486TM SX	Pentium	Pentium Pro	Pentium II
Introduced	1991	1993	1995	1997
Clock speeds	16 MHz–33 MHz	60 MHz–166 MHz,	150 MHz–200 MHz	200 MHz–300 MHz
Bus width	32 bits	32 bits	64 bits	64 bits
Number of transistors	1.185 million	3.1 million	5.5 million	7.5 million
Feature size (μm)	1	0.8	0.6	0.35
Addressable memory	4 GB	4 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	8 kB	8 kB	512 kB L1 and 1 MB L2	512 kB L2

(d) Recent Processors


	Pentium III	Pentium 4	Core 2 Duo	Core i7 EE 990
Introduced	1999	2000	2006	2011
Clock speeds	450–660 MHz	1.3–1.8 GHz	1.06–1.2 GHz	3.5 GHz
Bus width	64 bits	64 bits	64 bits	64 bits
Number of transistors	9.5 million	42 million	167 million	1170 million
Feature size (nm)	250	180	65	32
Addressable memory	64 GB	64 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	512 kB L2	256 kB L2	2 MB L2	1.5 MB L2/12 MB L3

Poslednjih 10tak godina



CPU | Caches | Mainboard | Memory | SPD | Graphics | Bench | About

Processor

Name	Intel Core i7 6700K				
Code Name	Skylake	Max TDP	95.0 W		
Package	Socket 1151 LGA				
Technology	14 nm	Core Voltage	1.320 V		
Specification	Intel(R) Core(TM) i7-6700K CPU @ 4.00GHz				
Family	6	Model	E	Stepping	3
Ext. Family	6	Ext. Model	5E	Revision	R0
Instructions	MMX, SSE, SSE2, SSE3, SSSE3, SSE4.1, SSE4.2, EM64T, VT-x, AES, AVX, AVX2, FMA3, TSX				

Clocks (Core #0)		Cache	
Core Speed	4397.84 MHz	L1 Data	4 x 32 KBytes 8-way
Multiplier	x 44.0 (8 - 44)	L1 Inst.	4 x 32 KBytes 8-way
Bus Speed	100.00 MHz	Level 2	4 x 256 KBytes 4-way
Rated FSB		Level 3	8 MBytes 16-way


Selection: Processor #1 Cores: 4 Threads: 8

CPU-Z Ver. 1.76.0.x64 Tools ▼ Validate Close

CPU Caches Mainboard Memory SPD Graphics Bench About

Processor

Name	Intel Core i9 7980XE		
Code Name	Skylake-X	Max TDP	165.0 W
Package	Socket 2066 LGA		
Technology	14 nm	Core Voltage	0.904 V



Specification: Intel® Core™ i9-7980XE CPU @ 2.60GHz (ES)

Family	6	Model	5	Stepping	4
Ext. Family	6	Ext. Model	55	Revision	H0

Instructions: MMX, SSE, SSE2, SSE3, SSSE3, SSE4.1, SSE4.2, EM64T, VT-x, AES, AVX, AVX2, AVX512F, FMA3, TSX

Clocks (Core #0)

Core Speed	3398.89 MHz
Multiplier	x 34.0 (12 - 42)
Bus Speed	99.97 MHz
Rated FSB	

Cache

L1 Data	18 x 32 KBytes	8-way
L1 Inst.	18 x 32 KBytes	8-way
Level 2	18 x 1 MBytes	16-way
Level 3	24.75 MBytes	11-way

Selection: Socket #1 Cores: 18 Threads: 36

CPU-Z Ver. 1.80.1.x64 Tools Validate Close

CPU-Z

CPU | Mainboard | Memory | SPD | Graphics | Bench | About

Processor

Name	Intel Core i9 13900K		
Code Name	Raptor Lake	Max TDP	125.0 W
Package	Socket 1700 LGA		
Technology	10 nm	Core Voltage	1.328 V
Specification	13th Gen Intel® Core™ i9-13900K		
Family	6	Model	7
Ext. Family	6	Ext. Model	B7
Stepping	1		
Revision	B0		
Instructions	MMX, SSE, SSE2, SSE3, SSSE3, SSE4.1, SSE4.2, EM64T, AES, AVX, AVX2, FMA3, SHA		

Clocks (P-Core #0)

Core Speed	5486.58 MHz
Multiplier	x 55.0 (8.0 - 55.0)
Bus Speed	99.76 MHz
Rated FSB	

Cache

L1 Data	8 x 48 KB + 16 x 32 KB
L1 Inst.	8 x 32 KB + 16 x 64 KB
Level 2	8 x 2 MB + 4 x 4 MB
Level 3	36 MBytes

Selection: Socket #1 | Cores: 8P + 16E | Threads: 32

CPU-Z Ver. 2.02.0.x64 | Tools | Validate | Close

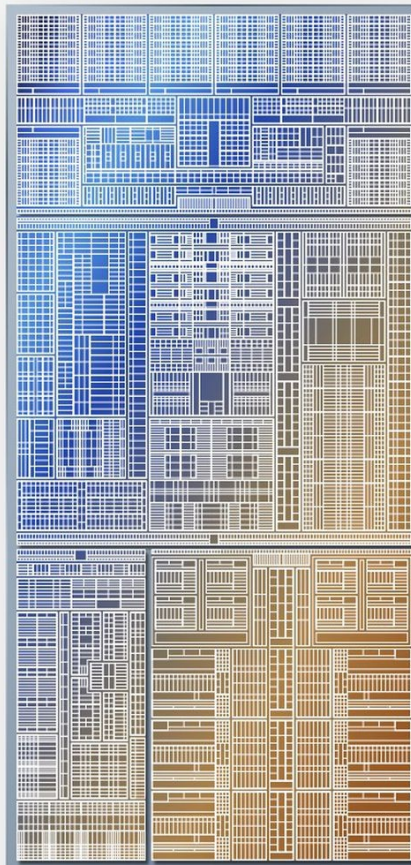
Meteor Lake

Industry leading **Wi-Fi 6E & Wi-Fi 7** support

Industry leading **FOVEROS 3D** packaging

Industry leading **Thunderbolt 4**

Latest connectivity **PCIe Gen5**



New Intel Arc graphics

New Media & Display standards

New Low power island E-cores

First Built-In NPU AI engine


First 3D performance hybrid architecture

New P-core & E-core microarchitectures

First on Intel 4 process technology


Intel's largest client SoC architectural shift in 40 years

Tu je i AMD

 CPU-Z - ID : ddjmgc

CPU | Caches | Mainboard | Memory | SPD | Graphics | Bench | About

Processor

Name	AMD Ryzen 9 5950X				
Code Name	Vermeer	Max TDP	105 W		
Package	Socket AM4 (1331)				
Technology	7 nm	Core Voltage	1.416 V		
Specification	AMD Ryzen 9 5950X 16-Core Processor				
Family	F	Model	1	Stepping	0
Ext. Family	19	Ext. Model	21	Revision	B0
Instructions	MMX(+), SSE, SSE2, SSE3, SSSE3, SSE4.1, SSE4.2, SSE4A, x86-64, AMD-V, AES, AVX, AVX2, FMA3, SHA				

Clocks (Core #0)

Core Speed	4723.9 MHz
Multiplier	x 47.25
Bus Speed	99.98 MHz
Rated FSB	

Cache

L1 Data	16 x 32 KBytes	8-way
L1 Inst.	16 x 32 KBytes	8-way
Level 2	16 x 512 KBytes	8-way
Level 3	2 x 32768 KBytes	16-way

Selection

Processor #1

Cores

16

Threads

32

CPU-Z

Ver. 1.96.1.x64

Tools

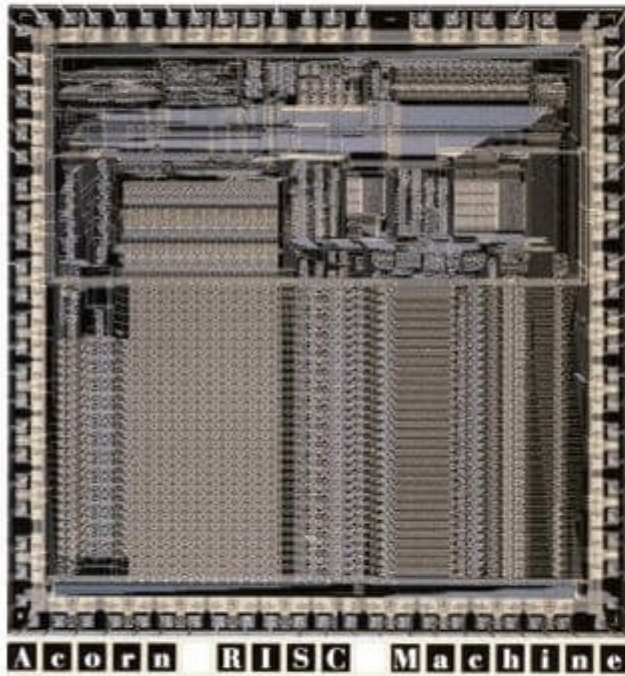
Validate

Close

ARM

Family	Notable Features	Cache	Typical MIPS @ MHz
ARM1	32-bit RISC	None	
ARM2	Multiply and swap instructions; Integrated memory management unit, graphics and I/O processor	None	7 MIPS @ 12 MHz
ARM3	First use of processor cache	4 kB unified	12 MIPS @ 25 MHz
ARM6	First to support 32-bit addresses; floating-point unit	4 kB unified	28 MIPS @ 33 MHz
ARM7	Integrated SoC	8 kB unified	60 MIPS @ 60 MHz
ARM8	5-stage pipeline; static branch prediction	8 kB unified	84 MIPS @ 72 MHz
ARM9		16 kB/16 kB	300 MIPS @ 300 MHz
ARM9E	Enhanced DSP instructions	16 kB/16 kB	220 MIPS @ 200 MHz
ARM10E	6-stage pipeline	32 kB/32 kB	
ARM11	9-stage pipeline	Variable	740 MIPS @ 665 MHz
Cortex	13-stage superscalar pipeline	Variable	2000 MIPS @ 1 GHz
XScale	Applications processor; 7-stage pipeline	32 kB/32 kB L1 512 kB L2	1000 MIPS @ 1.25 GHz

ARM

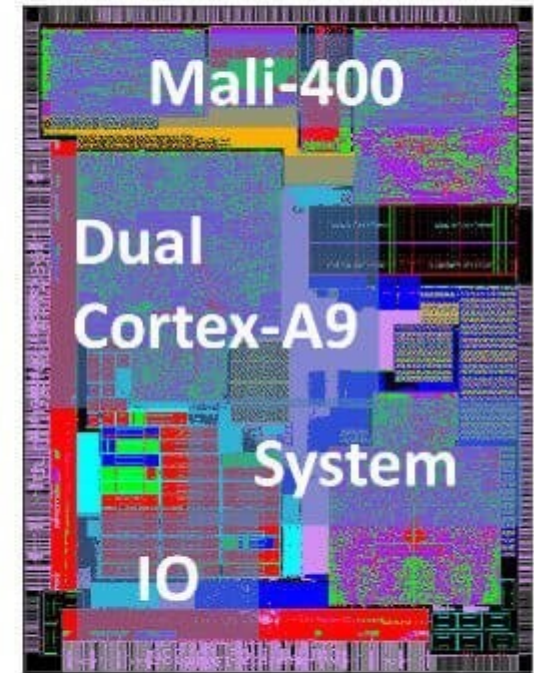


1985 ARM1
3 μ 6k gates
7mm x 7mm

1/10,000th
size



2010 Cortex-M0
20nm 8k gates
0.07mm x 0.07mm

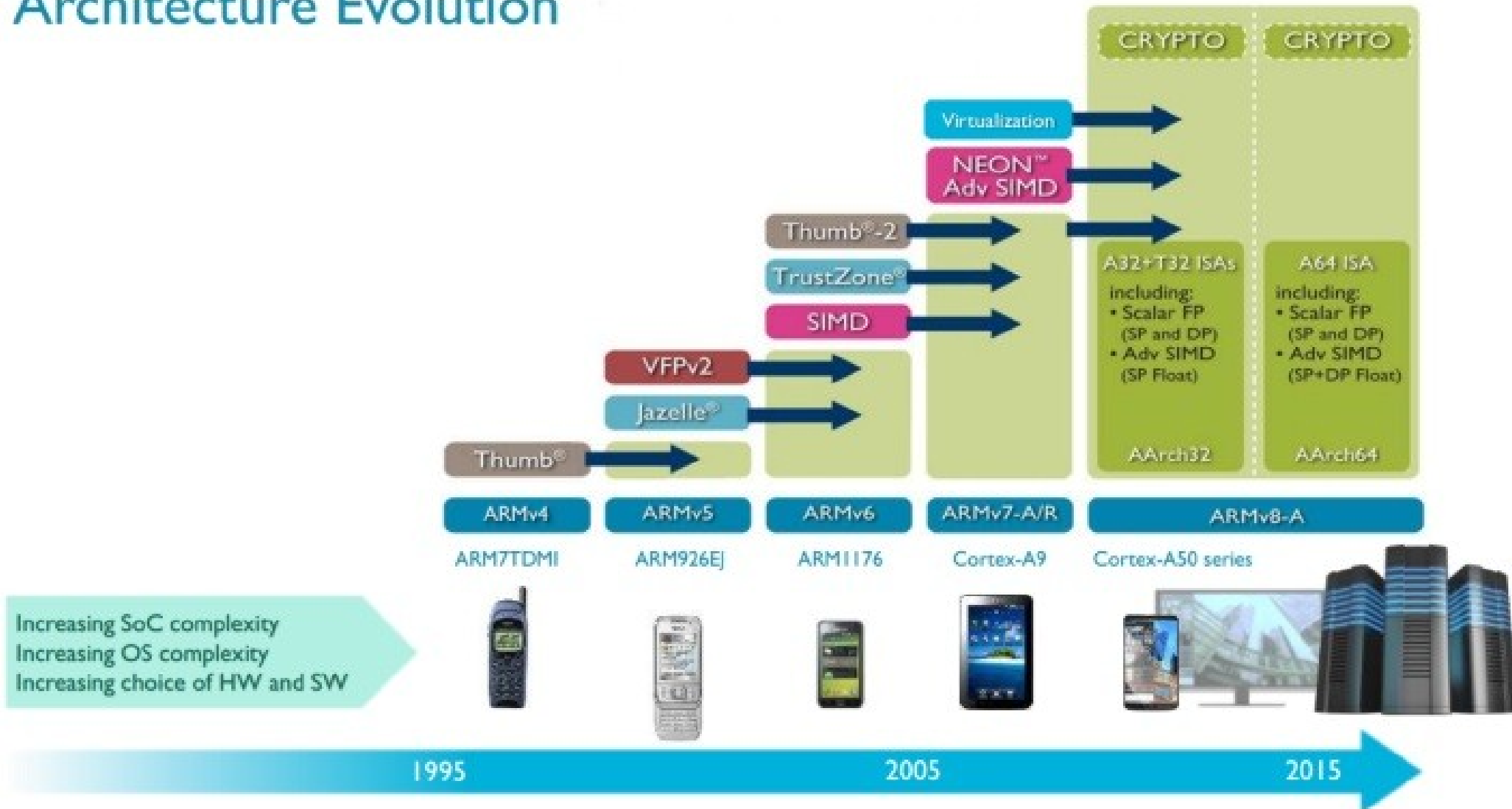


Cortex-A9 SOC
40nm 100M gates
7.4mm x 6.9mm

ARM



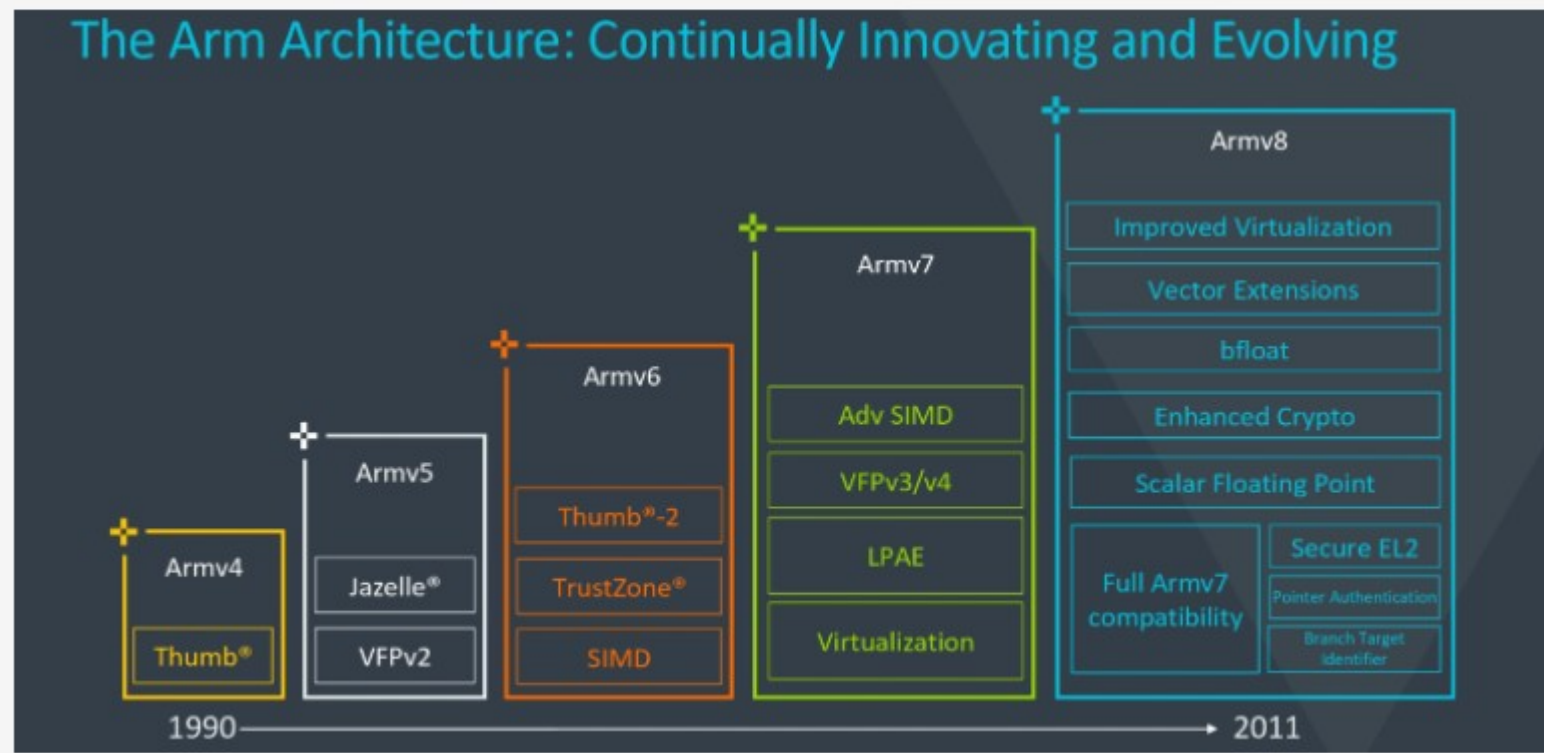
Architecture Evolution



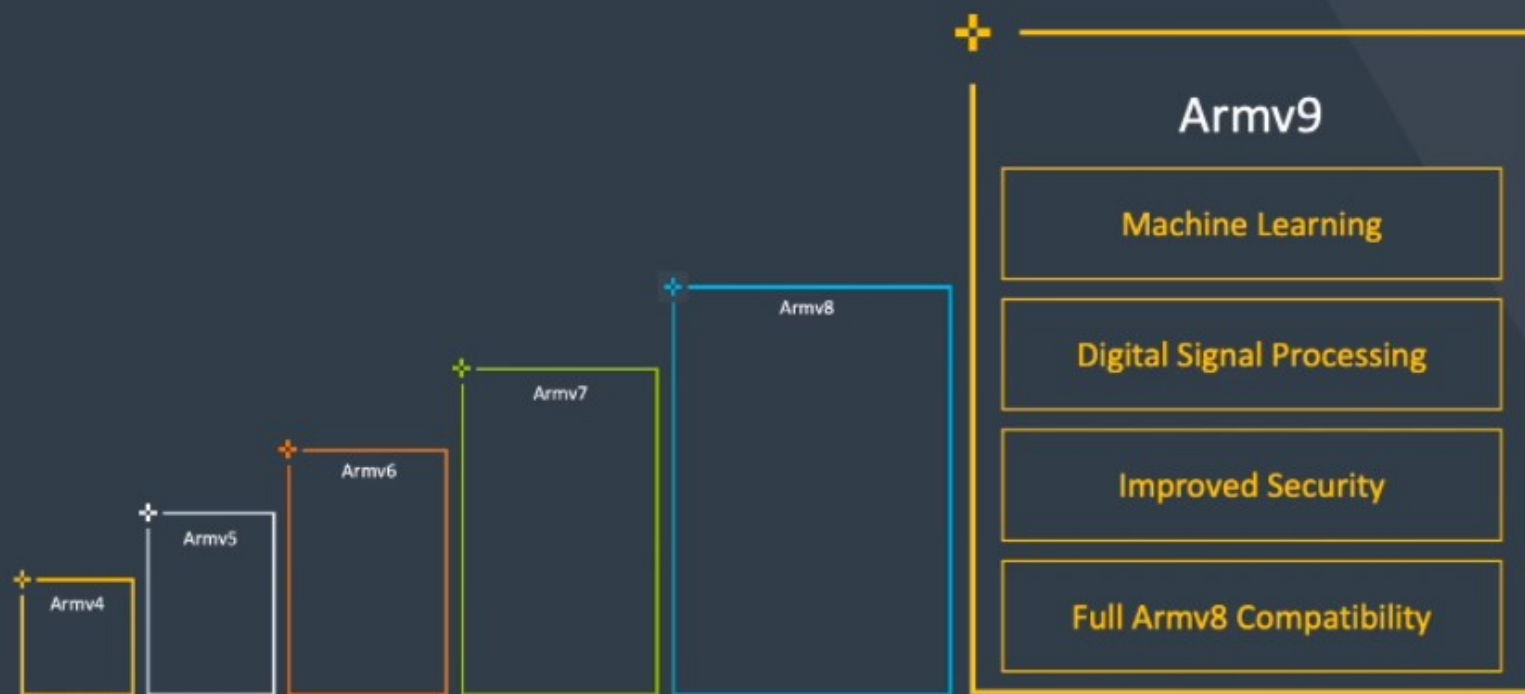
Arm Launches ARMv9

March 30, 2021 David Schor ARM, ARMv8, ARMv9, Confidential Compute Architecture (CCA), Scalable Vector Extension (SVE), Scalable Vector Extension 2 (SVE2)

Ten years ago Arm launched a new 64-bit architecture. ARMv8 more than just extended the virtual address space over ARMv7. It cleaned up and streamlined the architecture and eliminated legacy quirks. ARMv8 has proven to be an extremely successful architecture, adding numerous new features over the next decade. Today, Arm is launching its successor – ARMv9 for the next decade.



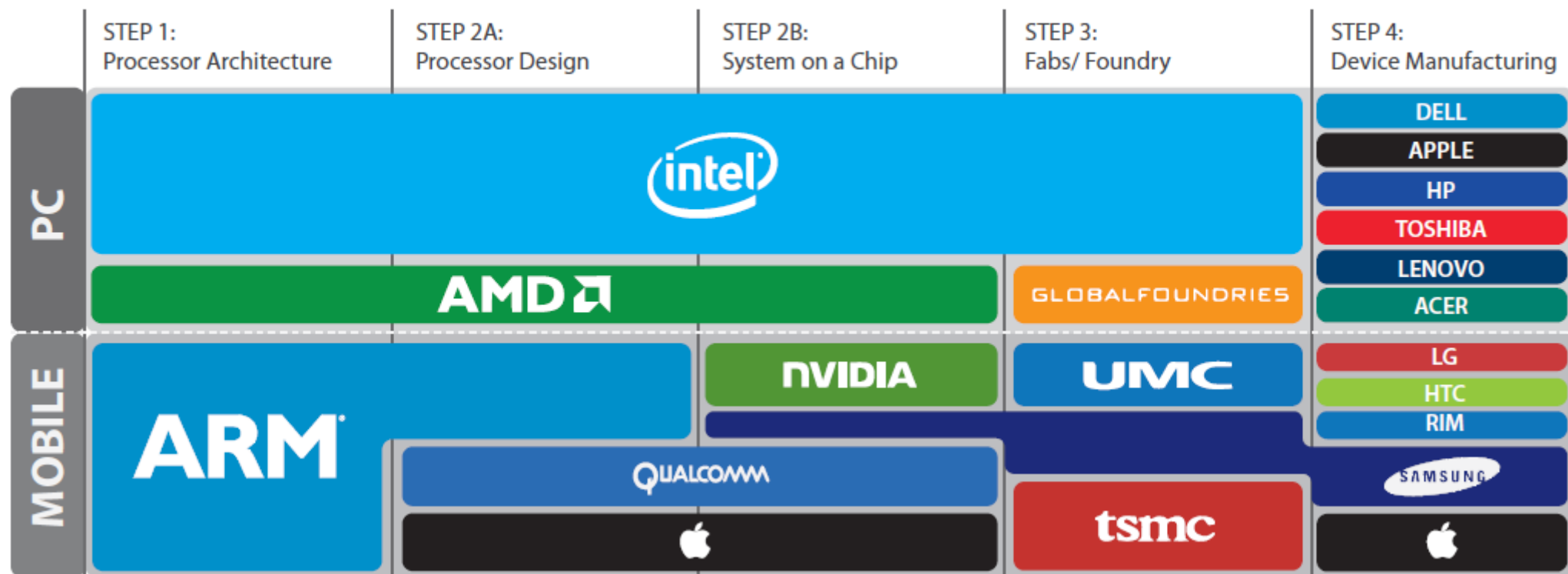
Introducing Armv9: The Secure Architecture for All Workloads



**Powering the next
300 billion chips**

Proizvodnja procesora

Processor Value Chain





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Press Release

NVIDIA to Acquire Arm for \$40 Billion, Creating World's Premier Computing Company for the Age of AI

Sunday, September 13, 2020



Intel & Arm Product

INTEL

- High End Powerful MicroProcessors
- Broad Product Range

Commonly Found in...

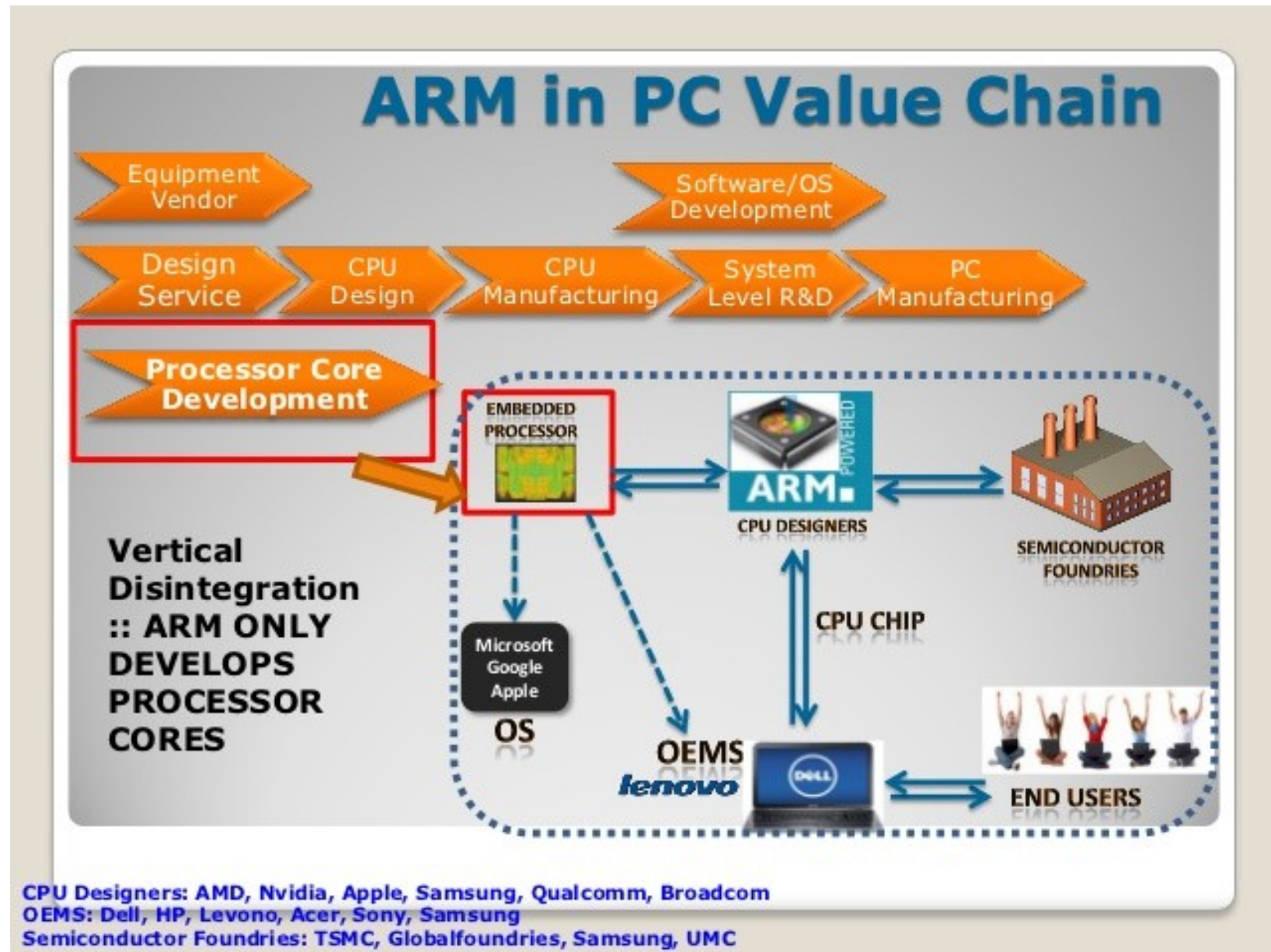


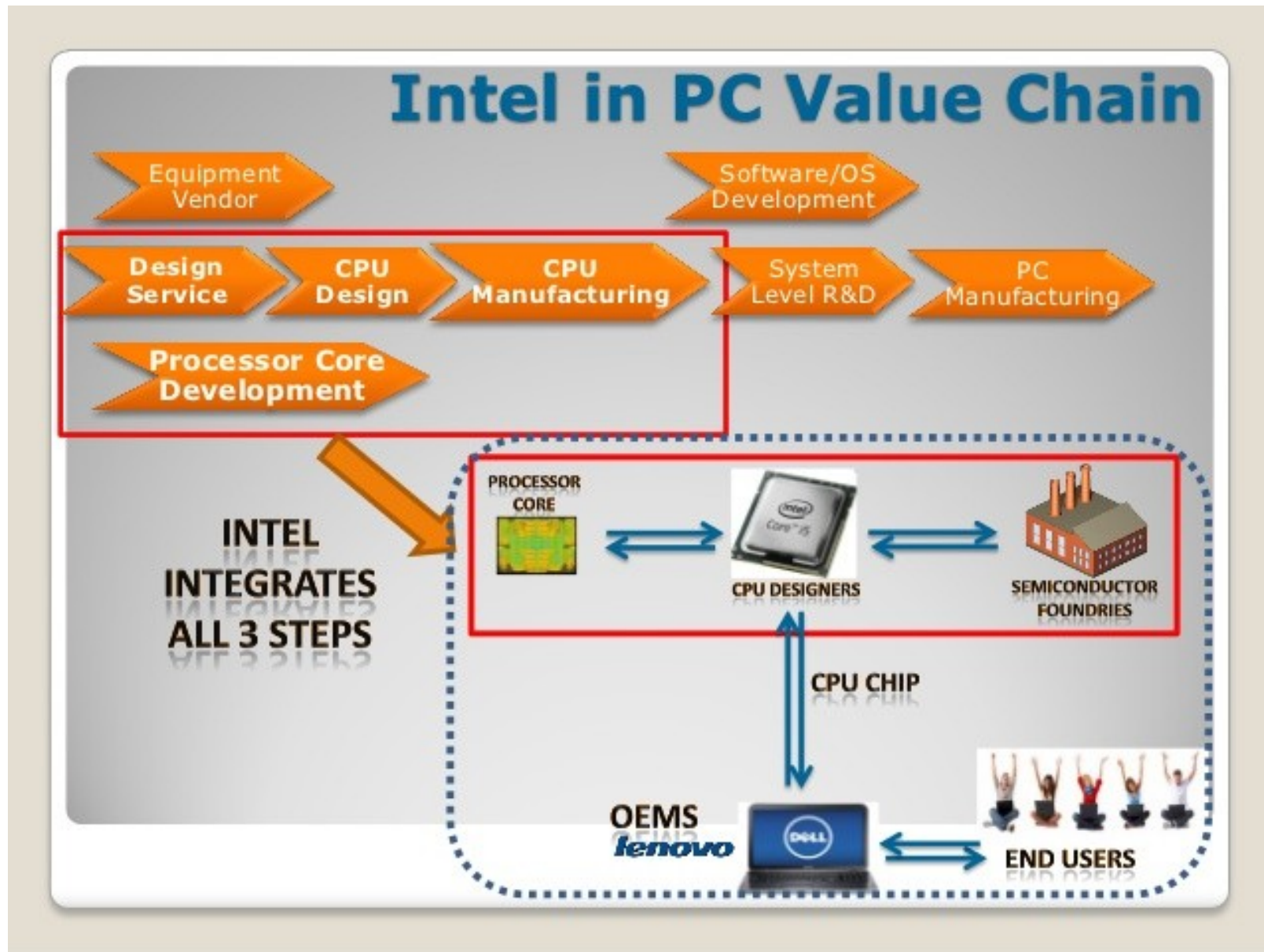
ARM

- Mobile Chips
- Small and Light
- Low Energy Consumption

Commonly Found in...







Zašto se učestanosti ne povećavaju?

Osećaj “saturacije” u oblasti proizvodnje procesora?

- zašto se učestanosti ne povećavaju
- memorija
- napon
- disipacija
- broj jezgara
- GPU

Osnovna arhitektura računara

1946-47.

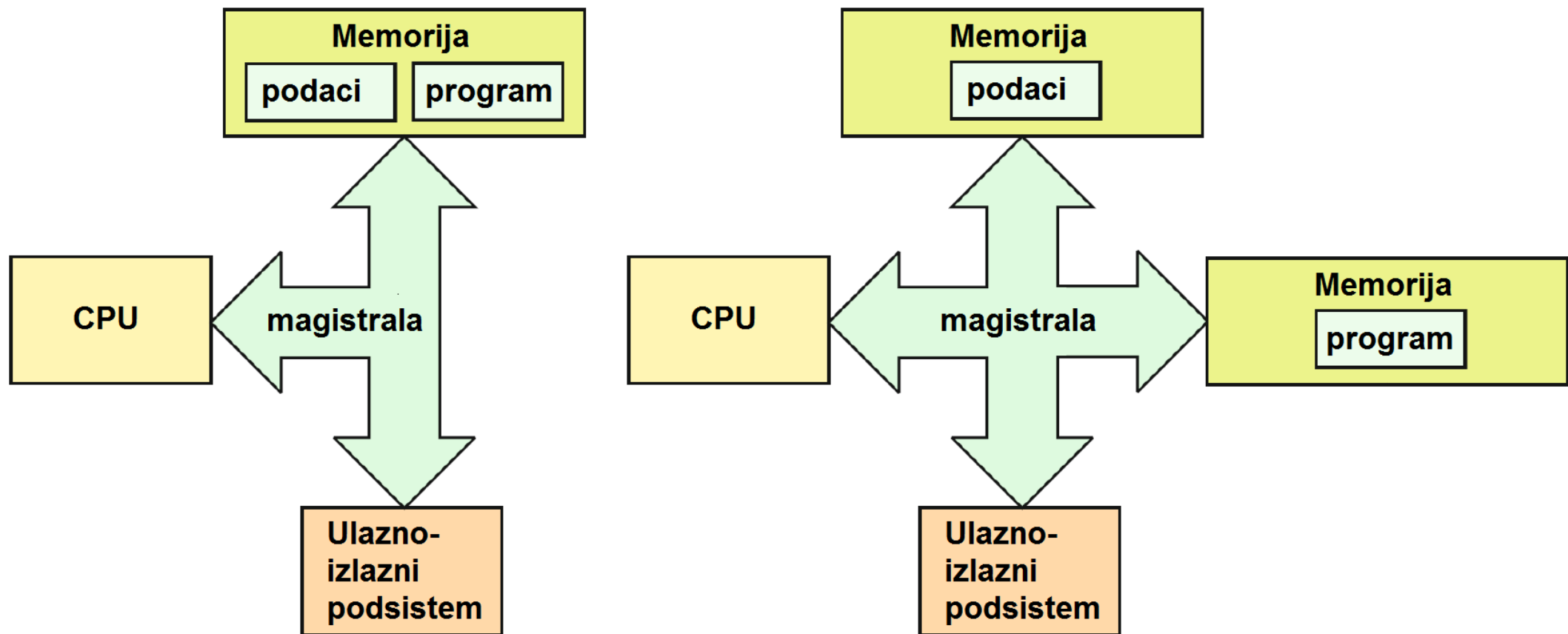
Preliminary discussion of the logical design of an electronic computer instrument

Burks, Arthur W. (Arthur Walter); Goldstine, Herman Heine; Von Neumann, John
1946

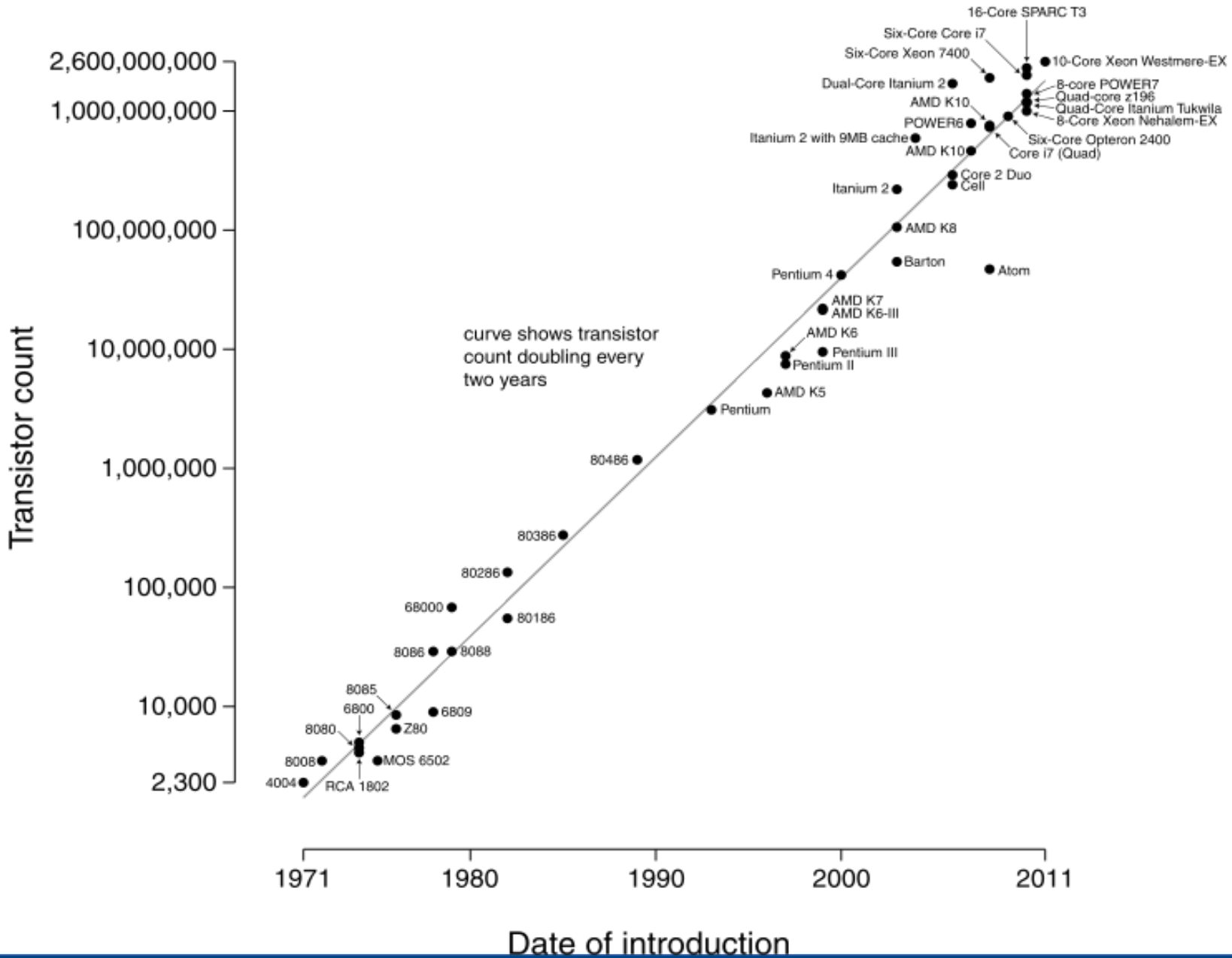
TABLE 1			
	SYMBOLIC		
	Complete	Abbreviated	
1.	$S(x) \rightarrow Ac+$	x	Clear accumulator and add number located at position x in the selectrons into it.
2.	$S(x) \rightarrow Ac-$	x -	Clear accumulator and subtract number located at position x in the selectrons into it.
3.	$S(x) \rightarrow AcM$	x M	Clear accumulator and add absolute value of number located at position x in the selectrons into it.
4.	$S(x) \rightarrow Ac-M$	x -M	Clear accumulator and subtract absolute value of number located at position x in the selectrons into it.
5.	$S(x) \rightarrow Ah+$	x h	Add number located at position x in the selectrons into the accumulator.
6.	$S(x) \rightarrow Ah-$	x h-	Subtract number located at position x in the selectrons into the accumulator.
7.	$S(x) \rightarrow AhM$	x hM	Add absolute value of number located at position x in the selectrons into the accumulator.
8.	$S(x) \rightarrow Ah-M$	x h-M	Subtract absolute value of number located at position x in the selectrons into the accumulator.
9.	$S(x) \rightarrow R$	x R	Clear register* and add number located at position x in the selectrons into it.
10.	$R \rightarrow A$	A	Clear accumulator and shift number held in register into it.
11.	$S(x) \times R \rightarrow A$	x X	Clear accumulator and multiply the number located at position x in the selectrons by the number in the register, placing the left-hand 39 digits of the answer in the accumulator and the right-hand 39 digits of the answer in the register.
12.	$A \div S(x) \rightarrow R$	x -	Clear register and divide the number in the accumulator by the number located in position x of the selectrons, leaving the remainder in the accumulator and placing the quotient in the register.
13.	$Cu \rightarrow S(x)$	x C	Shift the control to the left-hand order of the order pair located at position x in the selectrons.
14.	$Cu' \rightarrow S(x)$	x C'	Shift the control to the right-hand order of the order pair located at position x in the selectrons.
15.	$Cc \rightarrow S(x)$	x Cc	If the number in the accumulator is ≥ 0 , shift the control as in $Cu \rightarrow S(x)$.
16.	$Cc' \rightarrow S(x)$	x Cc'	If the number in the accumulator is ≥ 0 , shift the control as in $Cu' \rightarrow S(x)$.
17.	$At \rightarrow S(x)$	x S	Transfer the number in the accumulator to position x in the selectrons.
18.	$Ap \rightarrow S(x)$	x Sp	Replace the left-hand 12 digits of the left-hand order located at position x in the selectrons by the left-hand 12 digits in the accumulator.
19.	$Ap' \rightarrow S(x)$	x Sp'	Replace the left-hand 12 digits of the right-hand order located at position x in the selectrons by the left-hand 12 digits in the accumulator.
20.	L	L	Multiply the number in the accumulator by 2, leaving it there.
21.	R	R	Divide the number in the accumulator by 2, leaving it there.

* Register means arithmetic register.

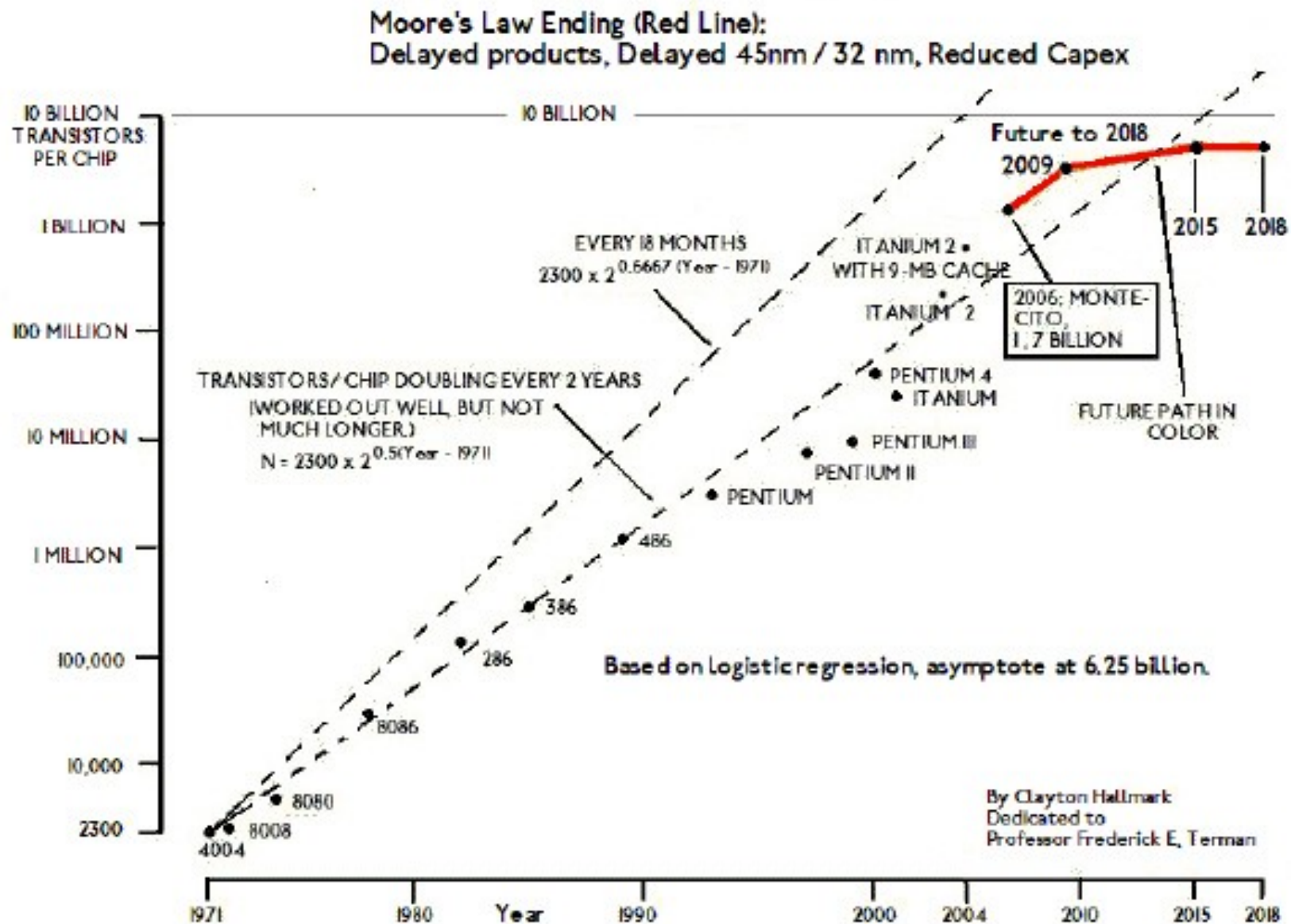
Osnovna arhitektura računara



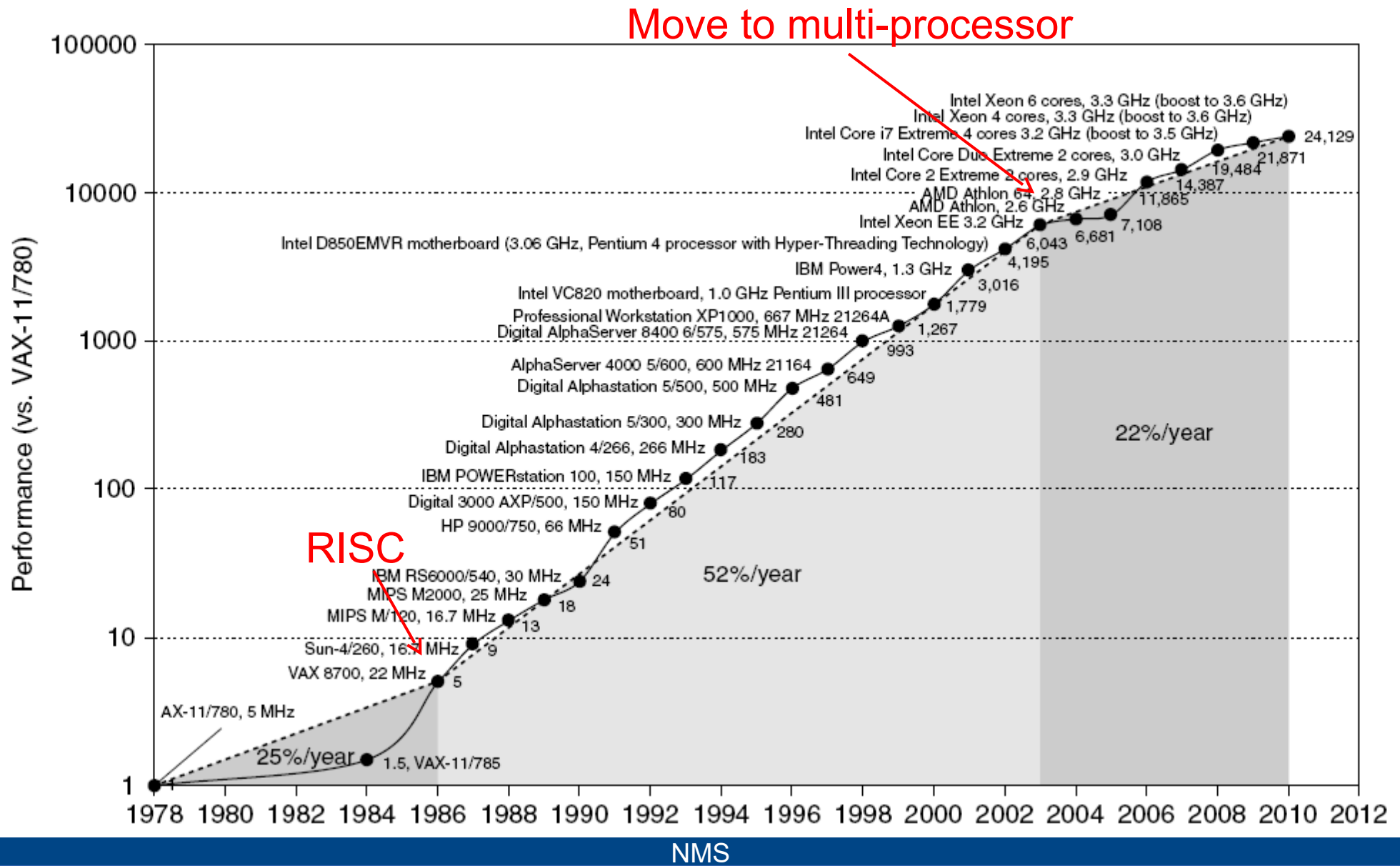
Microprocessor Transistor Counts 1971-2011 & Moore's Law



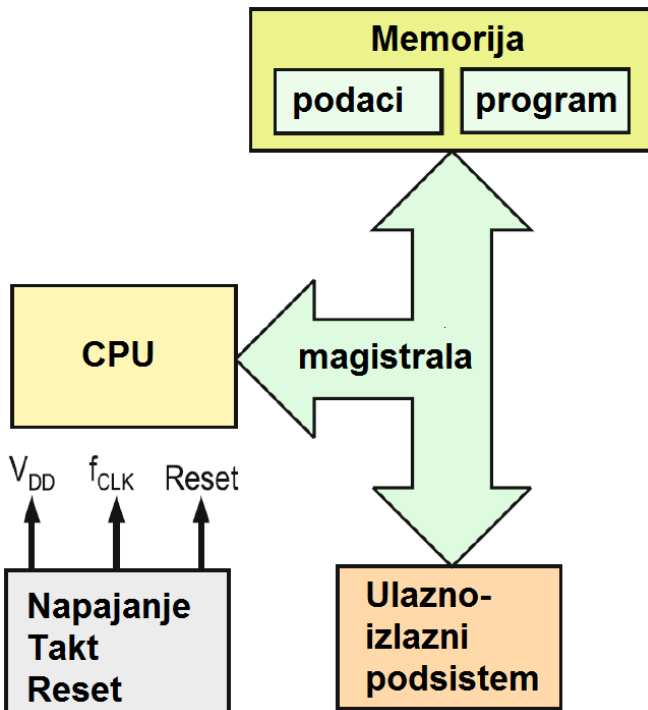
Moore's Law Ending?



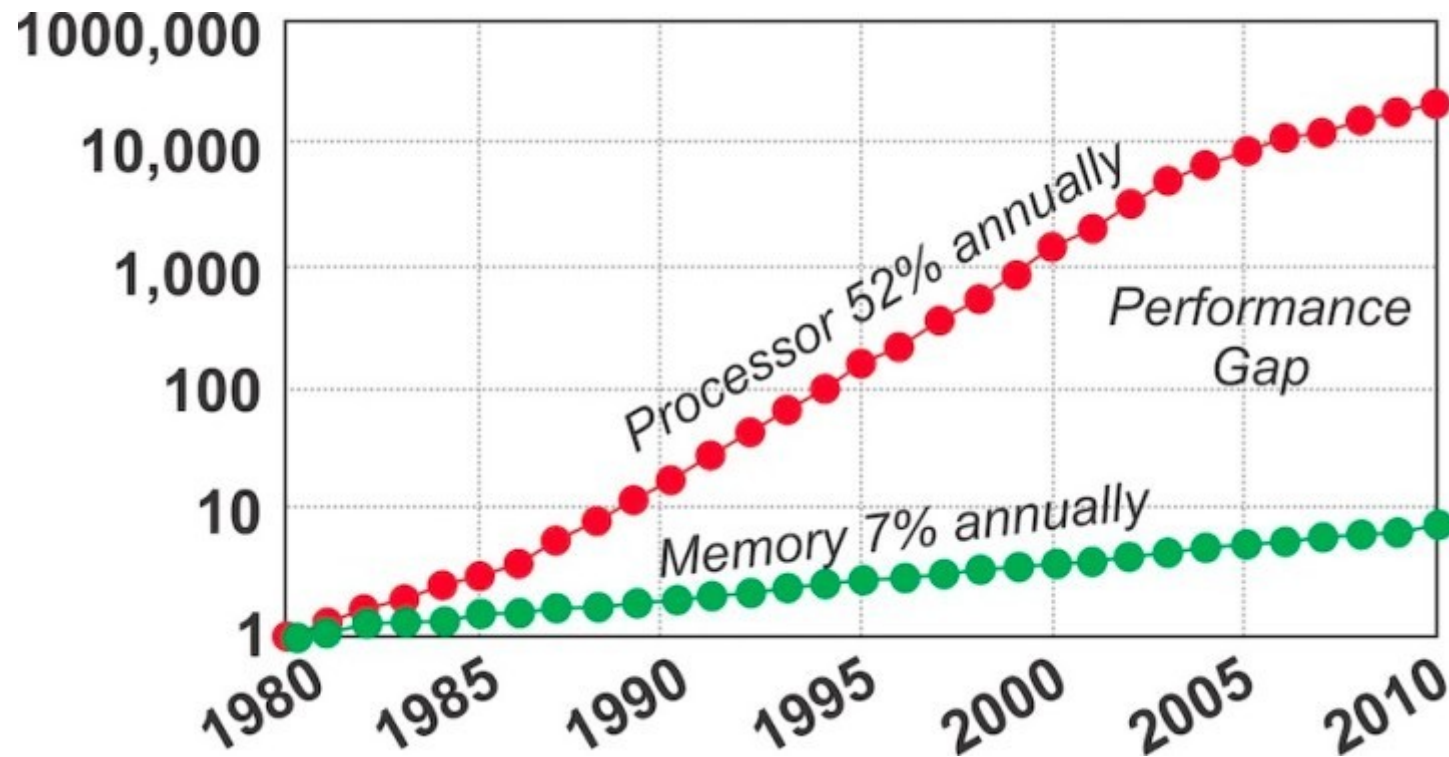
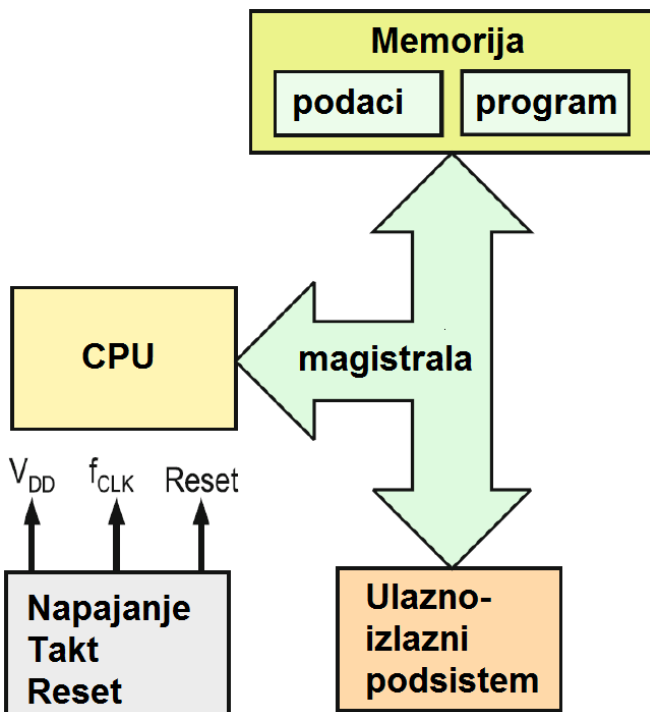
Single Processor Performance



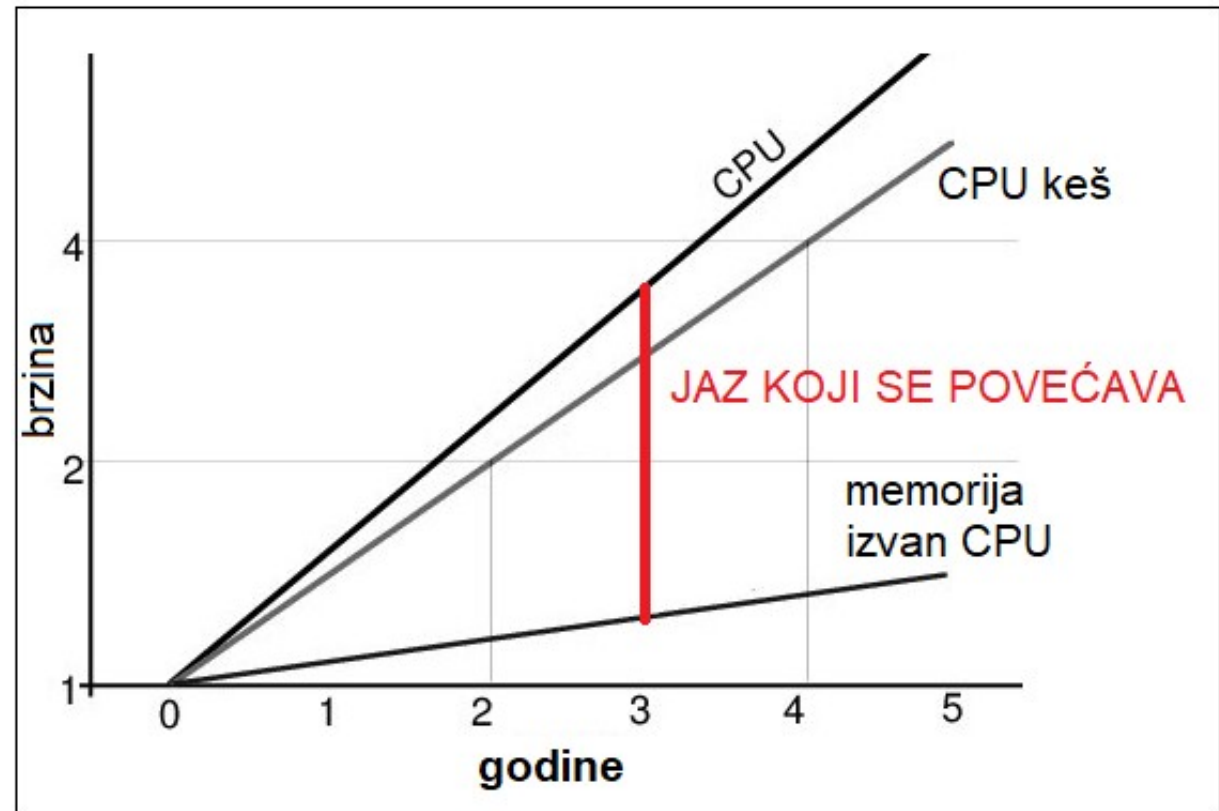
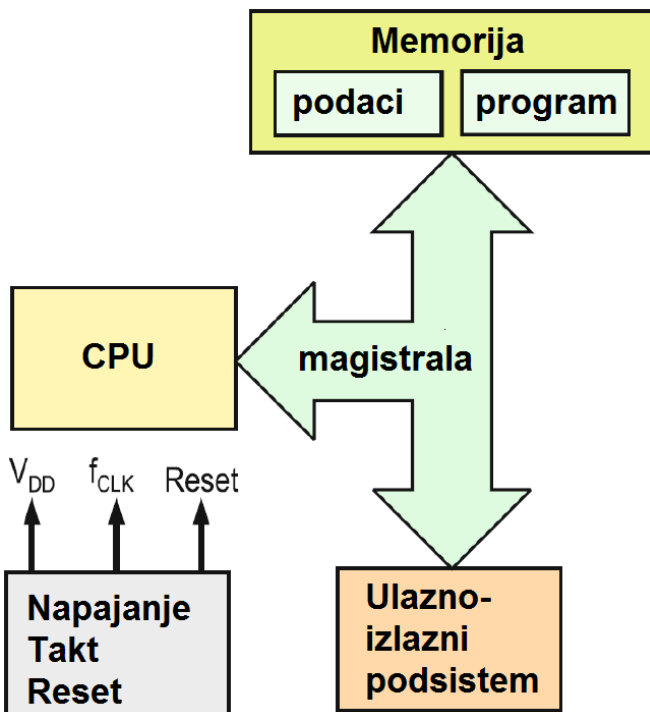
Memorijski “zid”



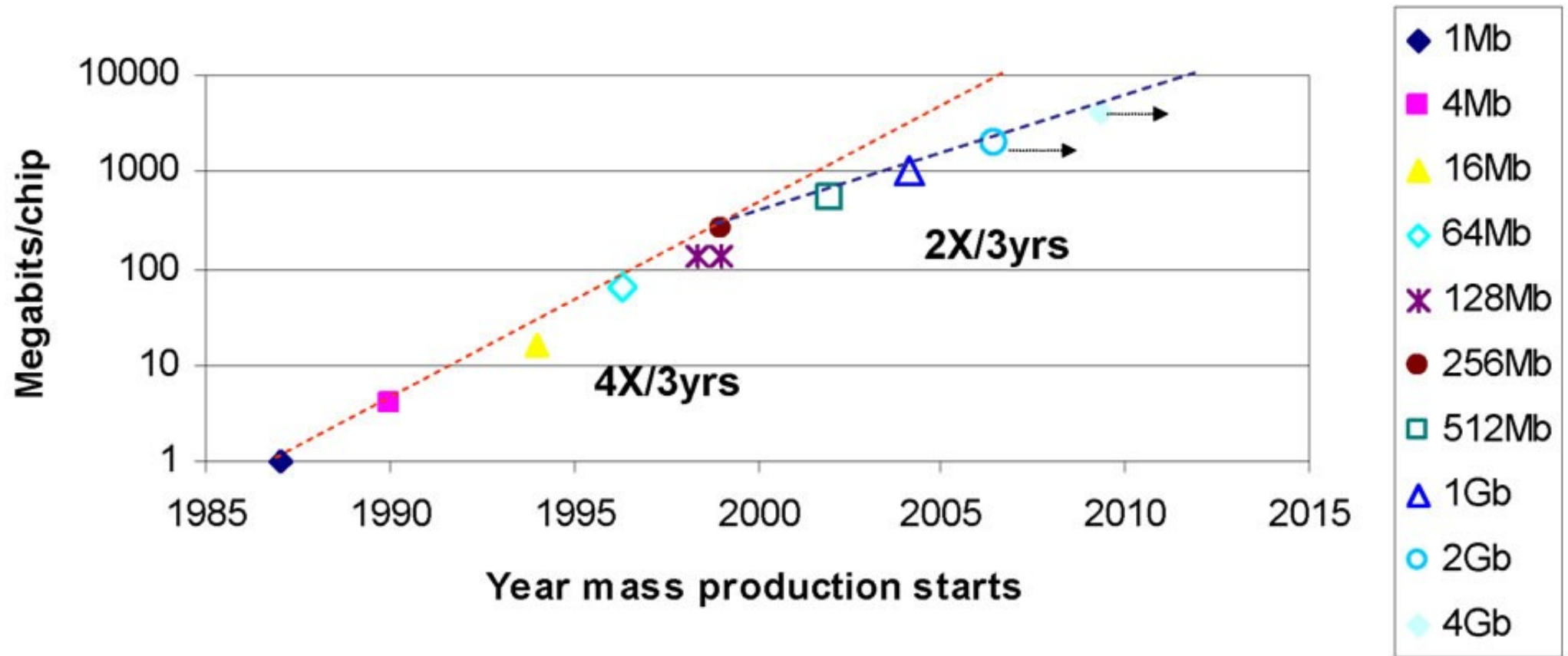
Memorijski “zid”



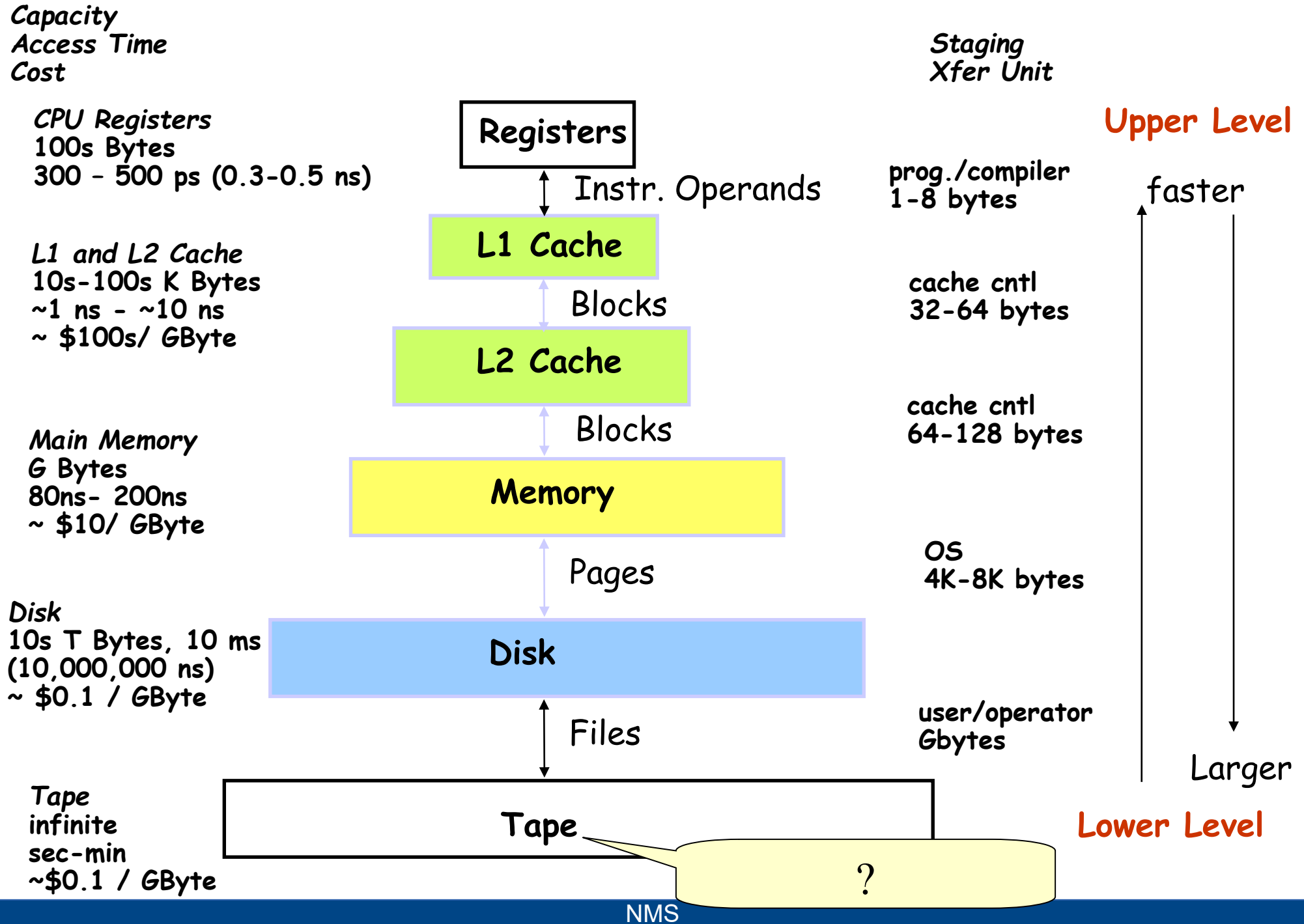
Memorijski “zid”



Evolution of memory granularity



Memorijska hijerarhija



Magnetne trake?

Three Advances Make Magnetic Tape More Than a Memory

Sony and IBM keep tape storage running apace, with these key developments

Posted 27 Sep 2017 | 15:00 GMT

By **PRACHI PATEL**

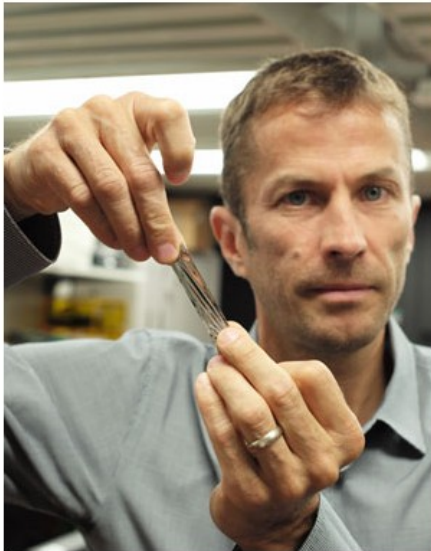


Photo: IBM Research

Small Tape, Big Cache: This 1-square-inch strip of magnetic tape, held by IBM Research's Mark Lantz, can store 201 gigabits of data, a new record.

In the age of flash memory and DNA-based data storage, magnetic tape sounds like an anachronism. But the workhorse storage technology is racing along. Scientists at IBM Research say they can now store 201 gigabits per square inch on a special “sputtered” tape made by Sony Storage Media Solutions.

The palm-size cartridge, into which IBM scientists squeezed a kilometer-long ribbon of tape, could hold 330 terabytes of data, or roughly 330 million books' worth. By comparison, the largest solid-state drive, made by Seagate, is twice as big and can store 60 TB, while the largest hard disk can store only 12 TB. IBM's best commercial tape cartridge, which began shipping this year, holds 15 TB.

<https://spectrum.ieee.org/computing/hardware/three-advances-make-magnetic-tape-more-than-a-memory>

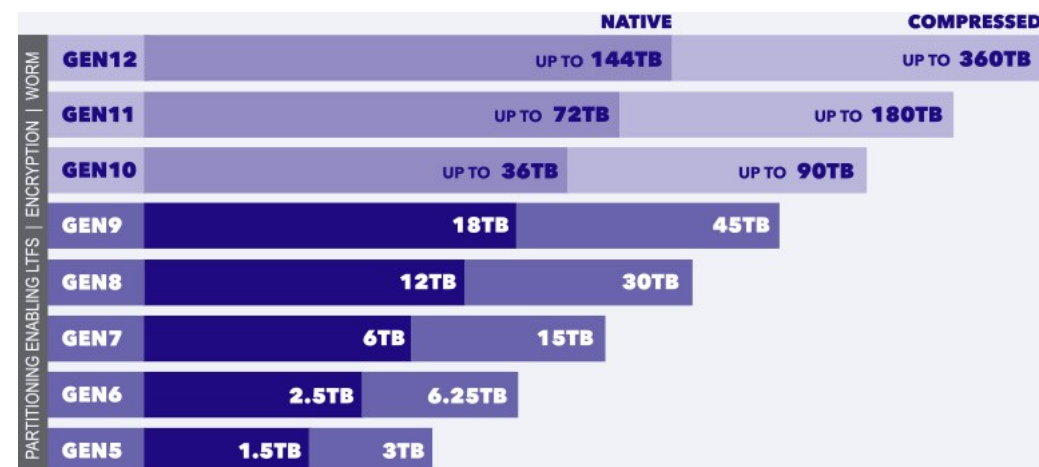
Ninth Generation Cyber Resilient Tape Storage for your hybrid cloud

Highlights

- Store up to 1EB per 18-frame library with 2.5:1 compression
- Achieve 18TB capacity per cartridge, 50% better than LTO 8
- Execute faster restores with 400MB/s transfer rate, 11% better than LTO 8
- Retrieve data 73% faster with Open RAO IBM LTO 9 Tape Drive technology

IBM LTO Ultrium Gen 9 tape technologies bring a new level of storage cost-efficiency and modern data protection to 21st century business.

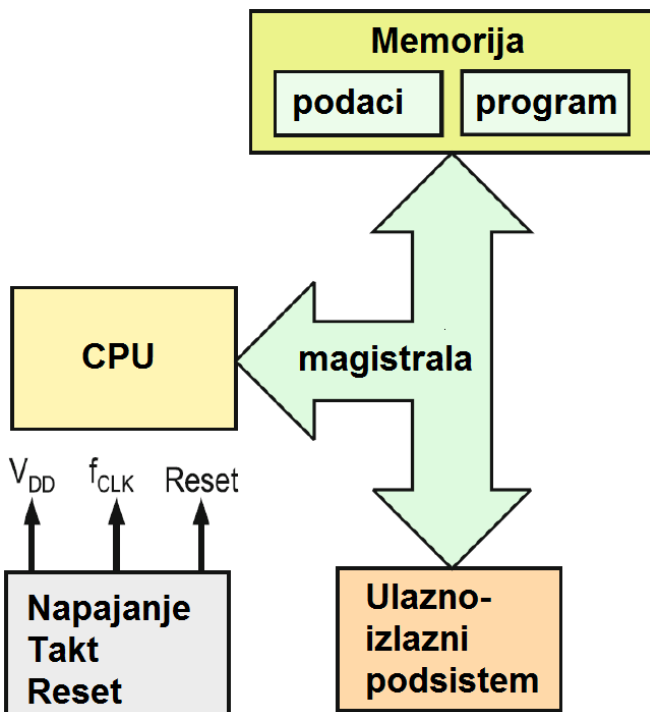
Two of the most powerful forces driving Information Technology (IT) today are the explosion of data volumes and the escalation of cyber security threats. Perhaps the fact that tape-based data storage solutions and technology have remained relevant and robust across the marketplace can be explained by how well tape addresses both of these critical issues.



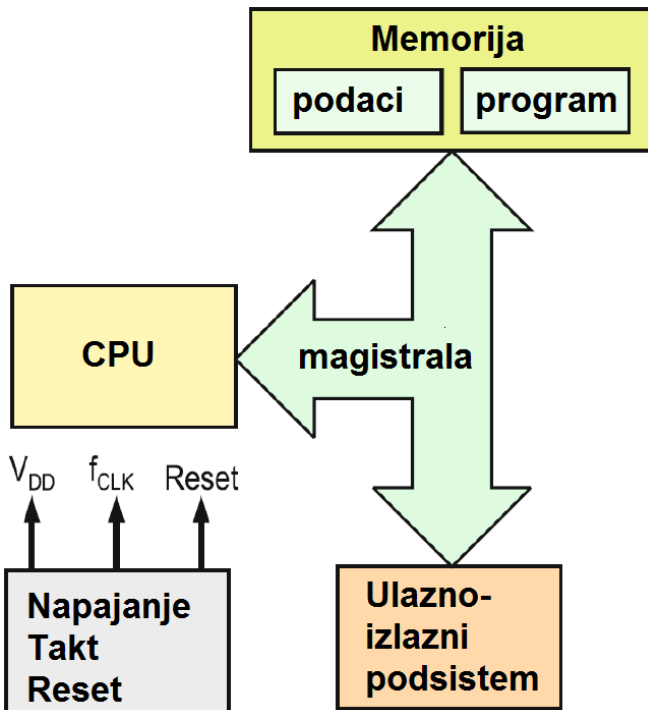
NOTE: Compressed capacity for generation 5 assumes 2:1 compression. Compressed capacities for generations 6-12 assume 2.5:1 compression (achieved with larger compression history buffer).

SOURCE: The LTO Program. The LTO Ultrium roadmap is subject to change without notice and represents goals and objectives only. Linear Tape-Open, LTO, the LTO logo, Ultrium, and the Ultrium logo are registered trademarks of Hewlett Packard Enterprise, International Business Machines Corporation and Quantum Corporation in the US and other countries.

“Zid snage” (*power wall*)



“Zid snage” (power wall)



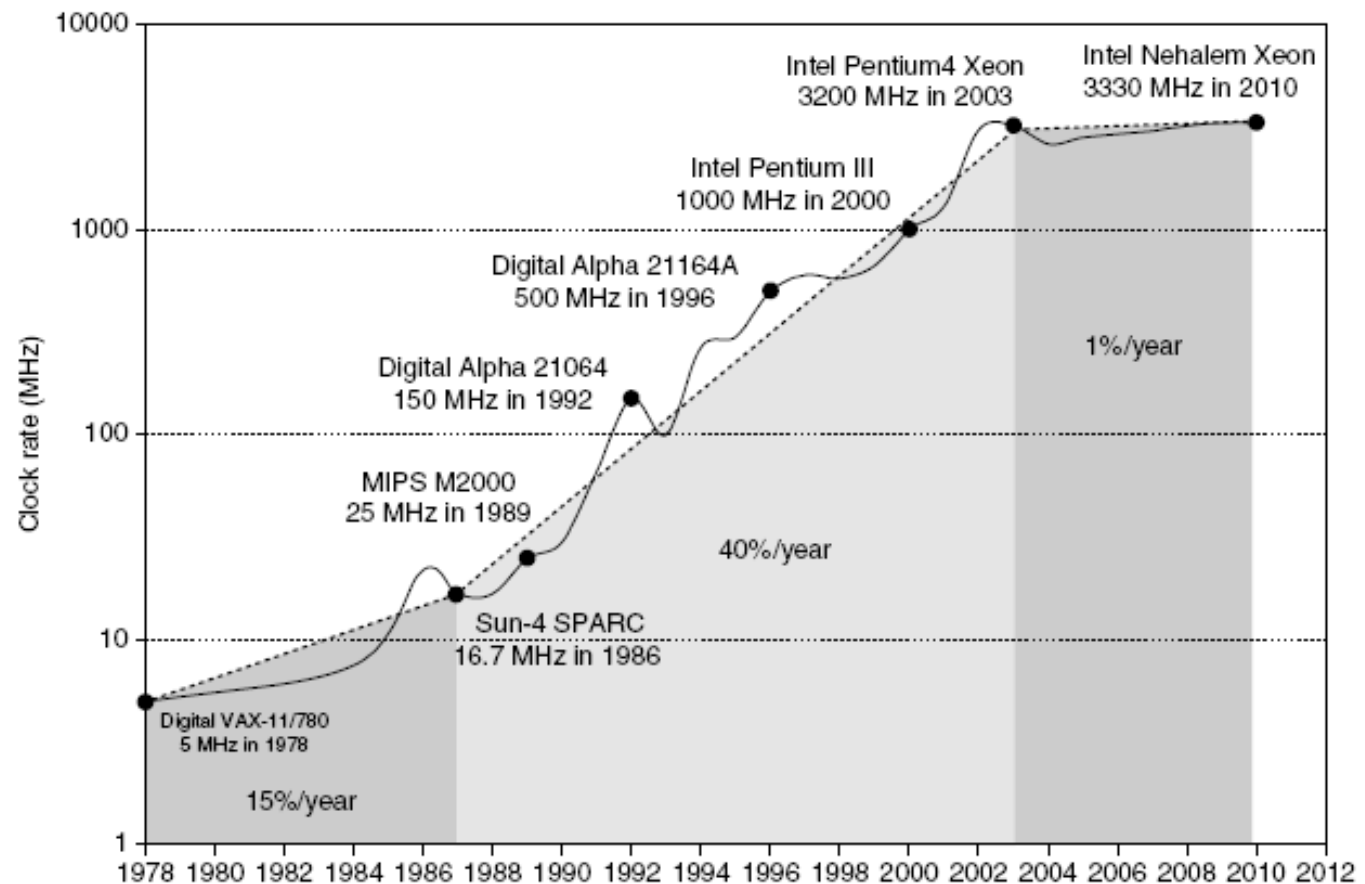
Disipacija snage je srazmerna:

$$P \sim a * C * f * V_{dd}^2$$

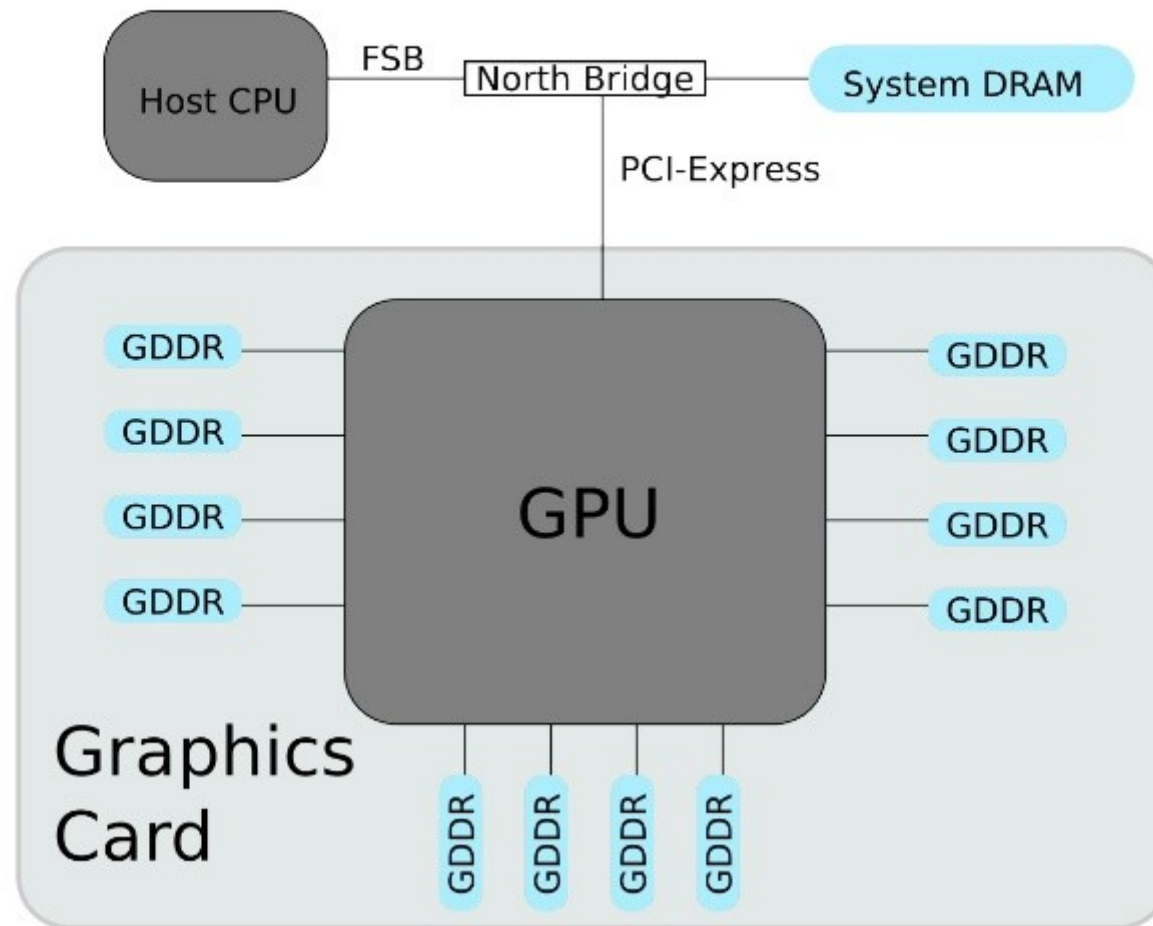
$$a \sim 1/2$$

Power

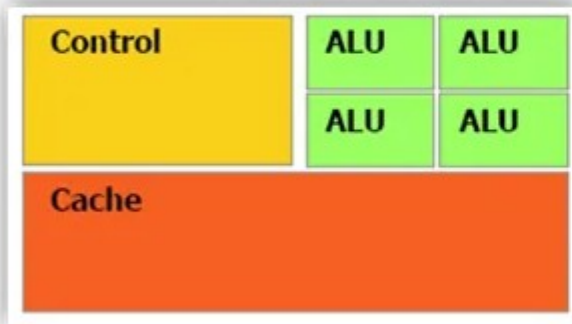
- Intel 80386 consumed ~ 2 W
- 3.3 GHz Intel Core i7 consumes 130 W
- Heat must be dissipated from 1.5 x 1.5 cm chip
- This is the limit of what can be cooled by air



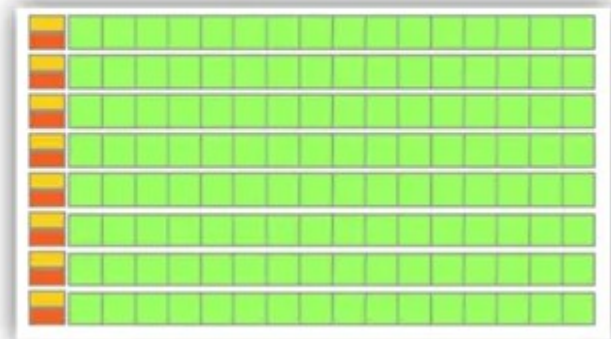
System Architecture



CPU

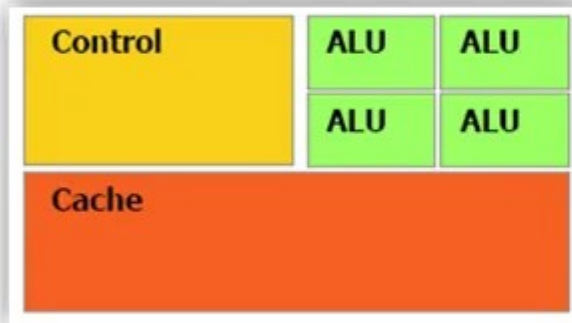


GPU



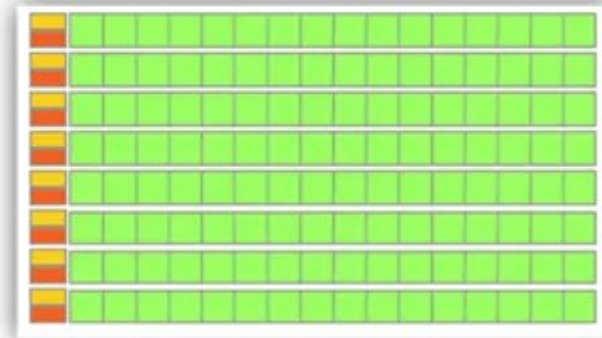
CPU - GPU

CPU



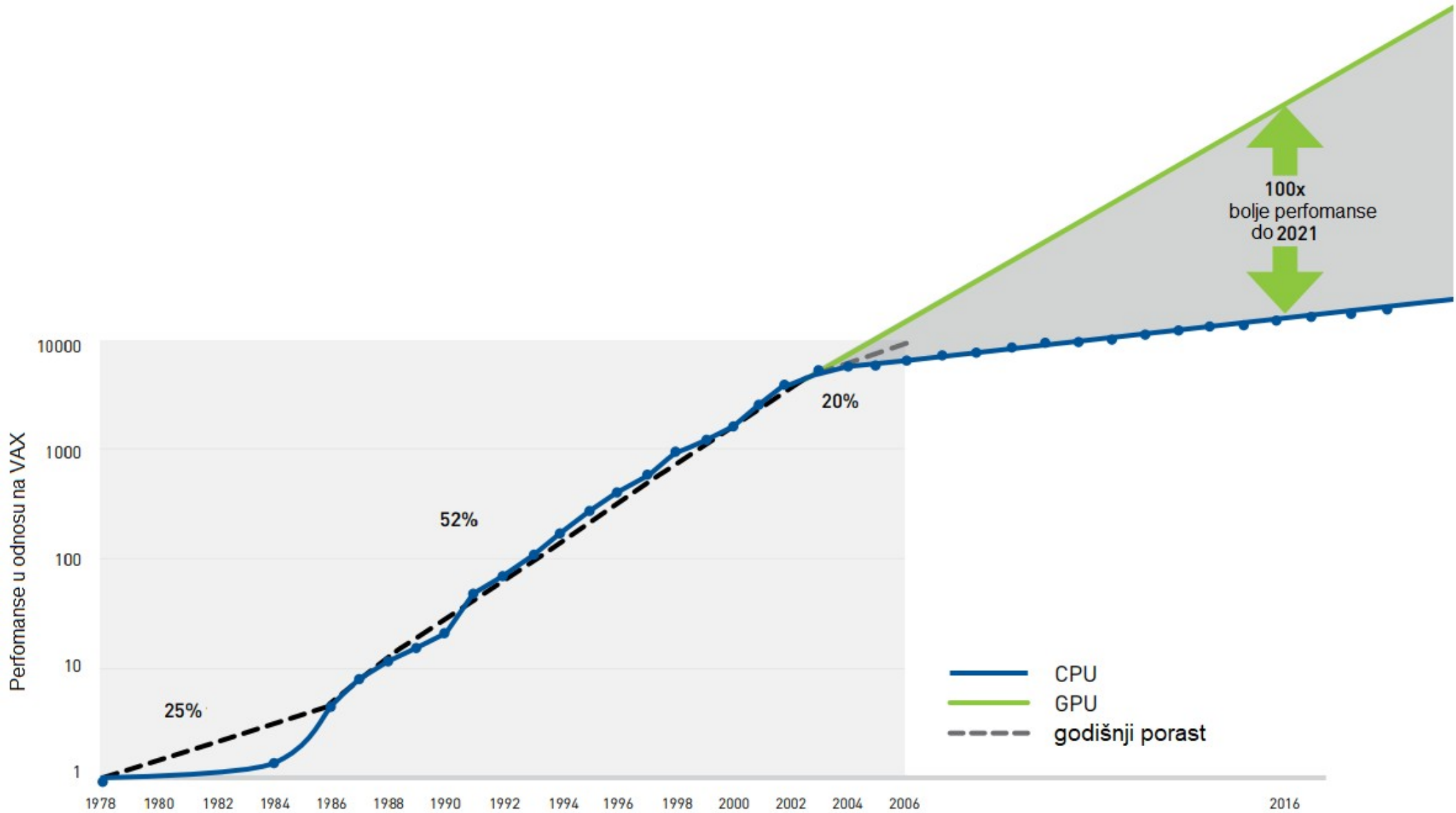
- * Low compute density
- * Complex control logic
- * Large caches (L1\$/L2\$, etc.)
- * Optimized for serial operations
 - Fewer execution units (ALUs)
 - Higher clock speeds
- * Shallow pipelines (<30 stages)
- * Low Latency Tolerance
- * Newer CPUs have more parallelism

GPU



- * High compute density
- * High Computations per Memory Access
- * Built for parallel operations
 - Many parallel execution units (ALUs)
 - Graphics is the best known case of parallelism
- * Deep pipelines (hundreds of stages)
- * High Throughput
- * High Latency Tolerance
- * Newer GPUs:
 - Better flow control logic (becoming more CPU-like)
 - Scatter/Gather Memory Access
 - Don't have one-way pipelines anymore

GPU



Neka (prelazna) rešenja?

Prelazno rešenje?



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News Release

December 28, 2015

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Contact Intel PR

INTEL COMPLETES ACQUISITION OF ALTERA

SANTA CLARA, Calif., Dec. 28, 2015 – Intel Corporation (“Intel”) today announced that it has completed the acquisition of Altera Corporation (“Altera”), a leading provider of field-programmable gate array (FPGA) technology. The acquisition complements Intel’s leading-edge product portfolio and enables new classes of products in the high-growth data center and Internet of Things (IoT) market segments.



“Altera is now part of Intel, and together we will make the next generation of semiconductors not only better but able to do more,” said Brian Krzanich, Intel CEO. “We will apply Moore’s Law to grow today’s FPGA business, and we’ll invent new products that make amazing experiences of the future possible – experiences like autonomous driving and machine learning.”

Altera will operate as a new Intel business unit called the Programmable Solutions Group (PSG), led by Altera veteran Dan McNamara. Intel is committed to a smooth transition for Altera customers and will continue the support and future product development of Altera’s many products, including FPGA, ARM[®]-based SoC and power products. In addition to strengthening the existing FPGA business, PSG will work closely with Intel’s Data Center Group and IoT Group to deliver the next generation of highly customized, integrated products and solutions.

“As part of Intel, we will create market-leading programmable logic devices that deliver a wider range of capabilities than customers experience today,” said McNamara, corporate vice president and general manager of the Programmable Solutions Group at Intel. “Combining Altera’s industry-leading FPGA technology and customer support with Intel’s world-class semiconductor manufacturing capabilities will enable customers to create the next generation of electronic systems with unmatched performance and power efficiency.”

Intel expects the acquisition to be accretive to non-GAAP EPS and free cash flow in the first full year after close, consistent with prior guidance. Intel expects the acquisition to be dilutive to GAAP EPS in the first full year after close primarily due to acquisition-related costs.

ARM is a registered trademark of ARM Limited (or its subsidiaries) in the European Union and/or elsewhere. All rights reserved.

Forward Looking Statements

This press release contains forward-looking statements, including statements concerning Altera’s development and sale of products and

Prelazno rešenje?

Intel® FPGAs and SoC FPGAs

Intel® FPGAs offer a wide variety of configurable embedded SRAM, high-speed transceivers, high-speed I/Os, logic blocks, and routing. Built-in intellectual property (IP) combined with outstanding software tools lower FPGA development time, power, and cost.



Intel Agilex® FPGA Portfolio

Built on Intel 10nm SuperFin and Intel 7 technology, enables customized acceleration.



Intel® Stratix® Series

Enables you to deliver high-end performance, state of the art products.



Intel® Arria® Series

Delivers Intel performance and power efficiency in the midrange.



Intel® MAX® Series

Featuring a unique, non-volatile architecture and deliver the market's best value.



Intel® Cyclone® FPGAs and SoC FPGAs

Built to meet your low-power, cost-sensitive design needs.



Intel® FPGA Configuration Devices

FPGA configuration devices from Intel are designed to support FPGA serial flash loader or ASMI parallel IP blocks.



[Home](#) > [Press Room](#)

Xilinx FPGAs to be Deployed in New Amazon EC2 F1 Instances - Accelerating Genomics, Financial Analytics, Video Processing, Big Data, Security, and Machine Learning Inference

Amazon EC2 F1 instances to include latest Xilinx 16nm UltraScale+ FPGAs

Dec 7, 2016

 [Photos \(1\)](#)

SAN JOSE, Calif., Dec. 7, 2016 /PRNewswire/ -- Xilinx, Inc. (NASDAQ:XLNX) today announced that Amazon Web Services (AWS) is deploying Xilinx 16nm UltraScale+™ Field Programmable Gate Arrays (FPGAs) in the new Amazon Elastic Cloud Compute (Amazon EC2) F1 instance type, accelerating genomics, financial analytics, video processing, big data, security, and machine learning inference workloads.

In addition to Amazon EC2 F1 instances, AWS also announced an FPGA Developer Amazon Machine Image (AMI), which is pre-built with the development tools and scripts including Xilinx's Vivado® Design Suite and Vivado license.

"We believe FPGAs are going mainstream in the cloud," said Steve Glaser, senior vice president, corporate strategy at Xilinx. "The AWS announcement last week is further evidence that this is happening right now and the momentum is building."

To learn more about the Amazon EC2 F1 instances web page at <https://aws.amazon.com/ec2/instance-types/f1/>, and AWS developer blog at <https://aws.amazon.com/blogs/aws/developer-preview-ec2-instances-f1-with-programmable-hardware/>.

About Xilinx

Xilinx is the leading provider of All Programmable FPGAs, SoCs, MPSoCs, and 3D ICs. Xilinx uniquely enables applications that are both software defined and hardware optimized – powering industry advancements in Cloud Computing, 5G Wireless, Embedded Vision, and Industrial IoT. For more information, visit www.xilinx.com.

AMD to Acquire Xilinx, Creating the Industry's High Performance Computing Leader

Share



— Strategic transaction strengthens AMD's industry-leading technology portfolio —

- Expands AMD's rapidly growing data center business
- Xilinx, the No. 1 provider of adaptive computing solutions, increases AMD TAM to \$110 billion
- Immediately accretive to AMD margins, cash flow and EPS
- All stock transaction with combined enterprise value of approximately \$135 billion

SILICON VALLEY, CALIF. 10/27/2020

AMD (NASDAQ: AMD) and Xilinx (NASDAQ: XLNX) today announced they have entered into a definitive agreement for AMD to acquire Xilinx in an all-stock transaction valued at \$35 billion. The combination will create the industry's leading high performance computing company, significantly expanding the breadth of AMD's product portfolio and customer set across diverse growth markets where Xilinx is an established leader. The transaction is expected to be immediately accretive to AMD margins, EPS and free cash flow generation and deliver industry-leading growth.

The acquisition brings together two industry leaders with complementary product portfolios and customers. AMD will offer the industry's strongest portfolio of high performance processor technologies, combining CPUs, GPUs, FPGAs, Adaptive SoCs and deep software expertise to enable leadership computing platforms for cloud, edge and end devices. Together, the combined company will capitalize on opportunities spanning some of the industry's most important growth segments from the data center to gaming, PCs, communications, automotive, industrial, aerospace and defense.

"Our acquisition of Xilinx marks the next leg in our journey to establish AMD as the industry's high performance computing leader and partner of choice for the largest and most important technology companies in the world," AMD President and CEO Dr. Lisa Su said. "This is truly a compelling combination that will create significant value for all stakeholders, including AMD and Xilinx shareholders who will benefit from the future growth and upside potential of the combined company. The Xilinx team is one of the strongest in the industry and we are thrilled to welcome them to the AMD family. By combining our world-class engineering teams and deep domain expertise, we will create an industry leader with the vision, talent and scale to define the future of high performance computing."

"We are excited to join the AMD family. Our shared cultures of innovation, excellence and collaboration make this an ideal combination. Together, we will lead the new era of high performance and adaptive computing," said Victor Peng, Xilinx president and CEO. "Our leading FPGAs, Adaptive SoCs, accelerator and SmartNIC solutions enable innovation from the cloud, to the edge and end devices. We empower our customers to deploy differentiated platforms to market faster, and with optimal efficiency and performance. Joining together with AMD will help accelerate growth in our data center business and enable us to pursue a broader customer base across more markets."

With a combined team of 13,000 talented engineers and over \$2.7 billion of annual¹ R&D investment, AMD will have additional talent and scale to deliver an even stronger set of products and domain-specific solutions.

AMD-Xilinx

Zynq™ 7000 SoC



Cost-Optimized Scalable SoC Platform

- Single or Dual Arm Cortex®-A9
- 28nm 7 Series Programmable Logic
- Up to 12.5G transceivers
- 7 Series Lifecycle Extended Through at Least 2035

Zynq 7000 SoC Devices

Zynq UltraScale+™ MPSoC



Industry's First Heterogeneous Adaptive SoC

- Dual or Quad Arm Cortex-A53
- Dual Arm Cortex-R5F
- 16nm FinFET+ Programmable Logic
- Arm Mali™-400MP2
- H.264/H.265 Video Codec

Zynq UltraScale+ MPSoC Devices

Zynq UltraScale+ RFSoc



Industry's First Single-Chip Adaptive Radio Platform

- Quad Arm Cortex-A53
- Dual Arm Cortex-R5F
- 16nm FinFET+ Programmable Logic
- Digital RF-ADC, RF-DAC, SD-FEC

Zynq UltraScale+ RFSoc Devices

Versal™ Adaptive SoC



Adaptive SoC

- Dual Arm Cortex-A72
- Dual Arm Cortex-R5F
- 7nm Programmable Logic
- DSP and AI Engines
- Programmable Network on Chip

Versal Adaptive SoC Devices

AMD-Xilinx

16nm

The combination of TSMC's 16nm FinFET process with new UltraRAM and SmartConnect technologies enables AMD to continue delivering 'More than Moore's Law' value to the market.

AMD
ARTIX
UltraScale+

AMD
KINTEX
UltraScale+

AMD
VIRTEX
UltraScale+

20nm

AMD enhanced FPGA architecture that contains a step-function increase in both the amount of connectivity resources and the associated inter-die bandwidth in this second-generation 3D IC architecture.

AMD
KINTEX
UltraScale

AMD
VIRTEX
UltraScale

28nm

Continuous innovation on the process node enables new devices with optimal performance at the lower power across product families to meet requirements for key applications.

AMD
SPARTAN⁷

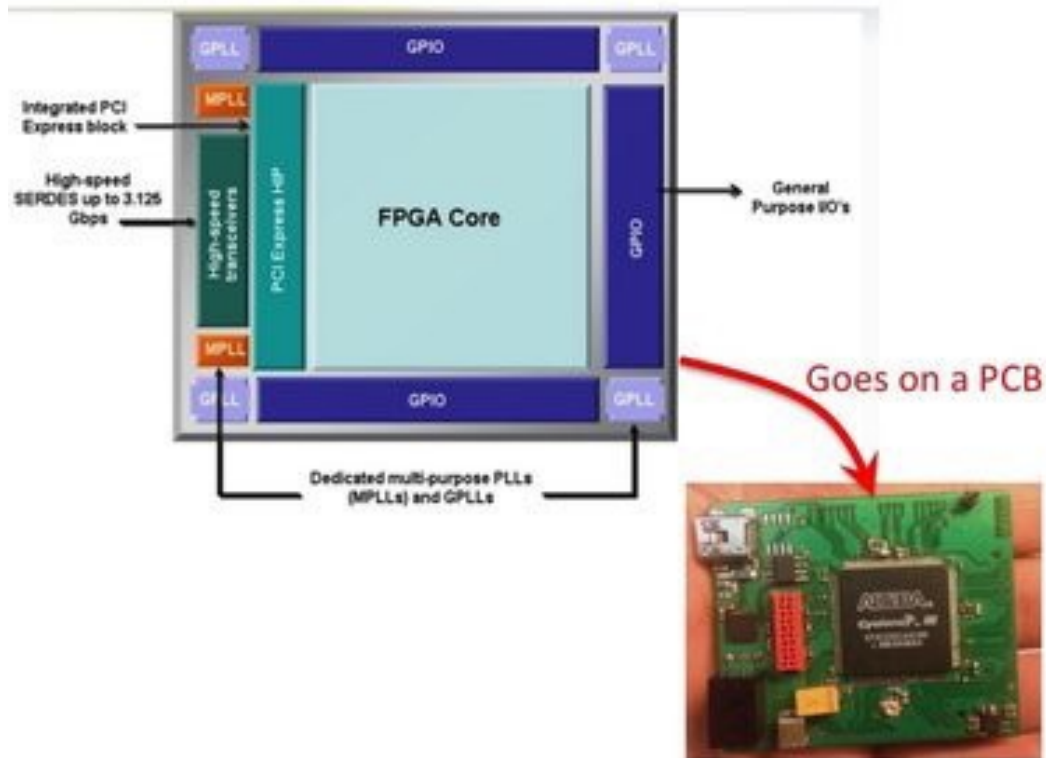
AMD
ARTIX⁷

AMD
KINTEX⁷

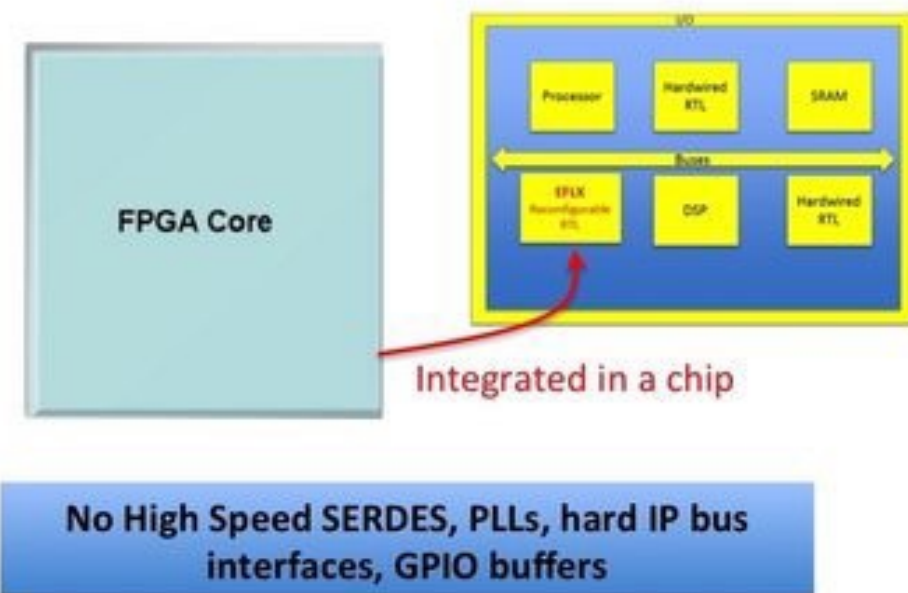
AMD
VIRTEX⁷

eFPGA

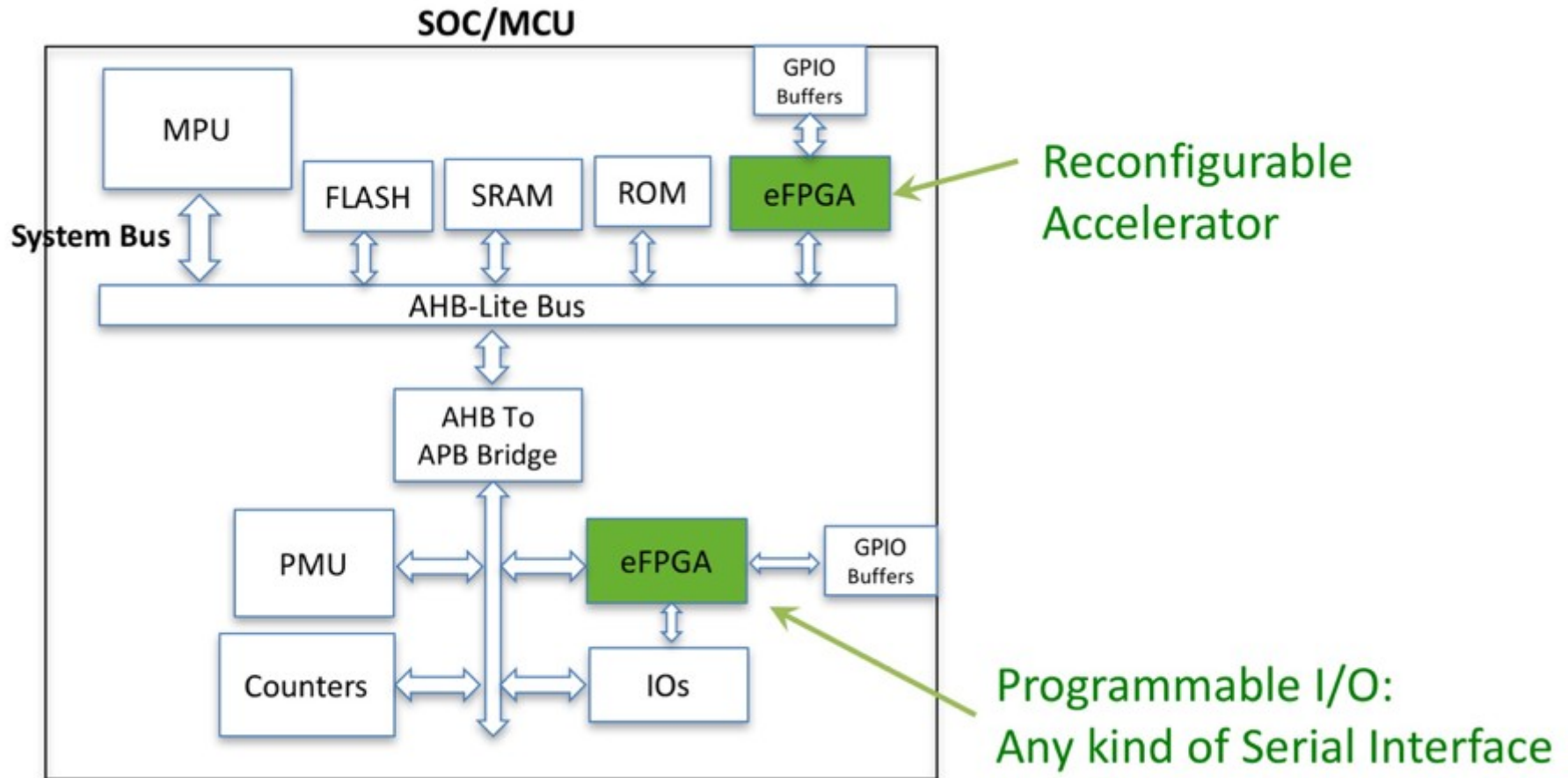
Typical FPGA Chip
(Altera Cyclone IV)



Embedded FPGA

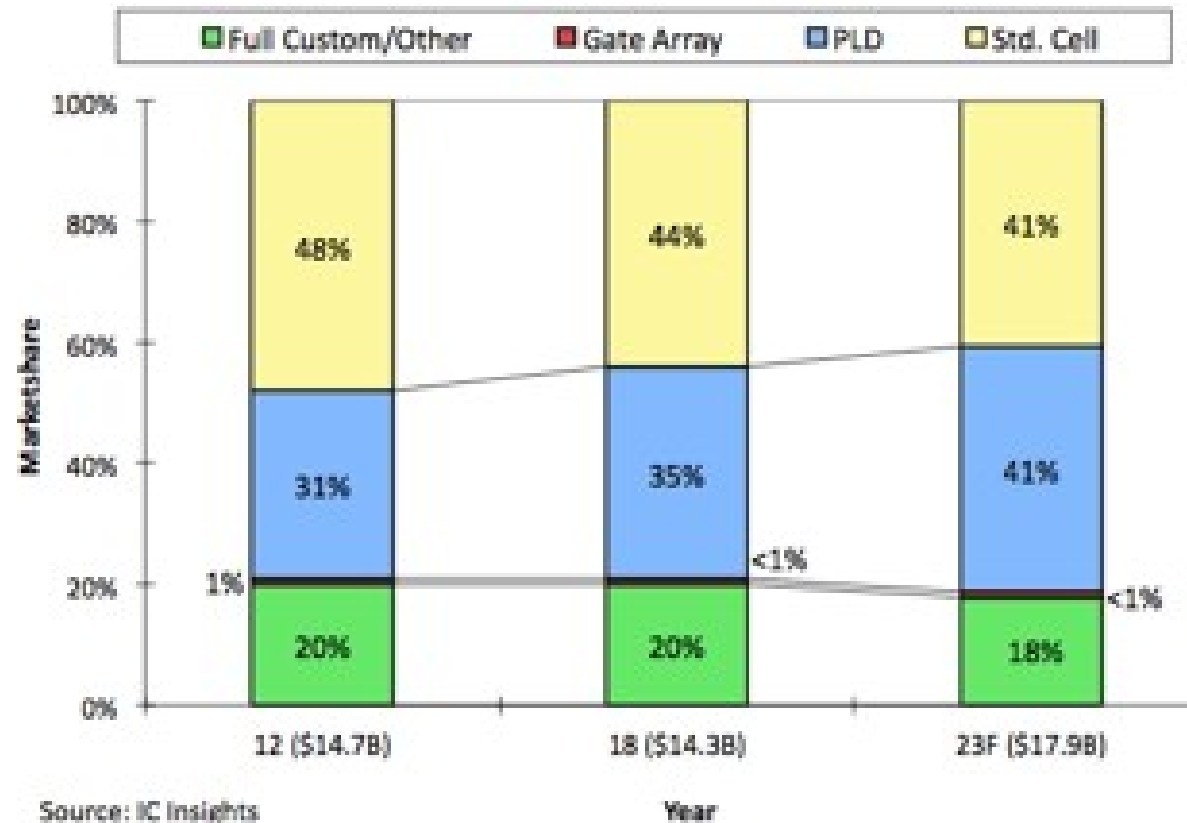


eFPGA



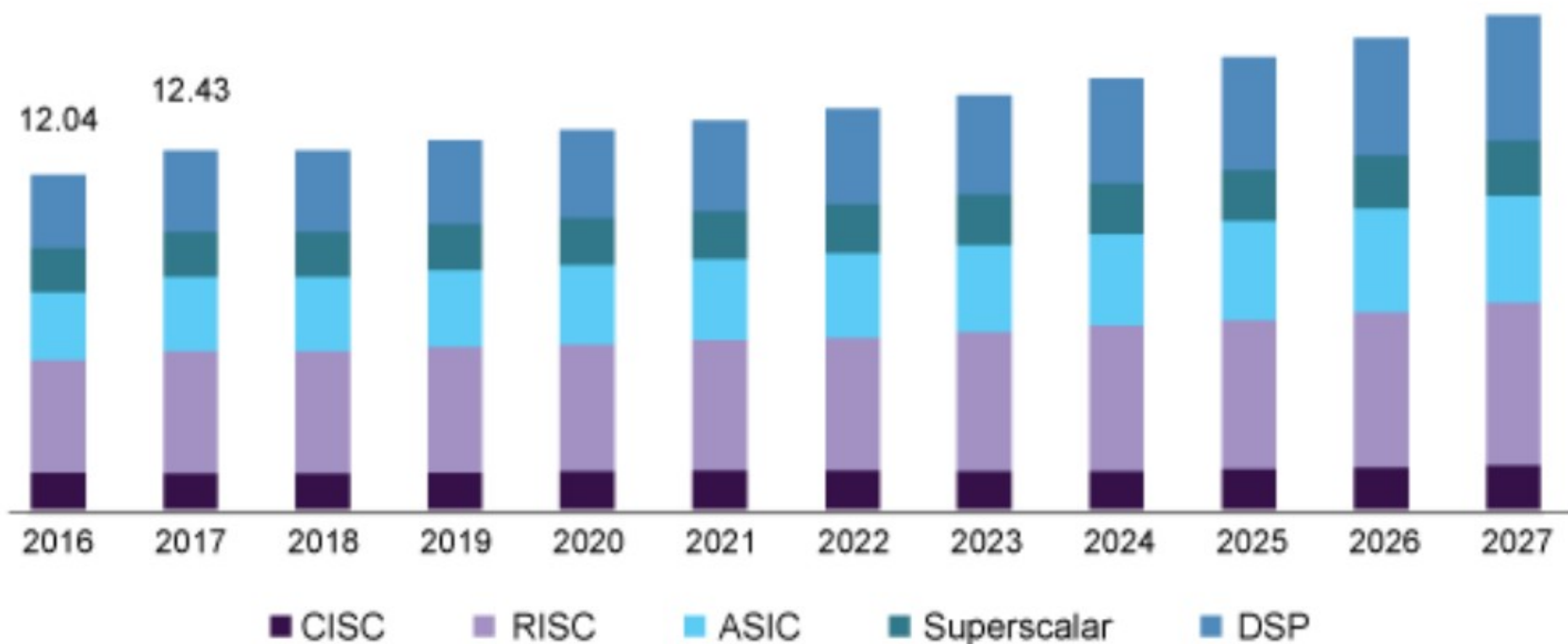
PLD - SoC

ASIC Product Segment Marketshare



MPU

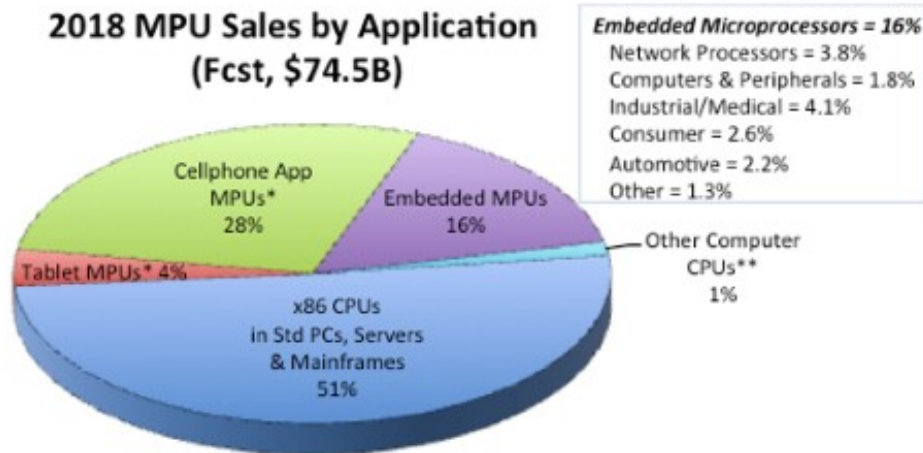
North America microprocessor market size,
by technology, 2016 - 2027 (USD Billion)



Source: www.grandviewresearch.com

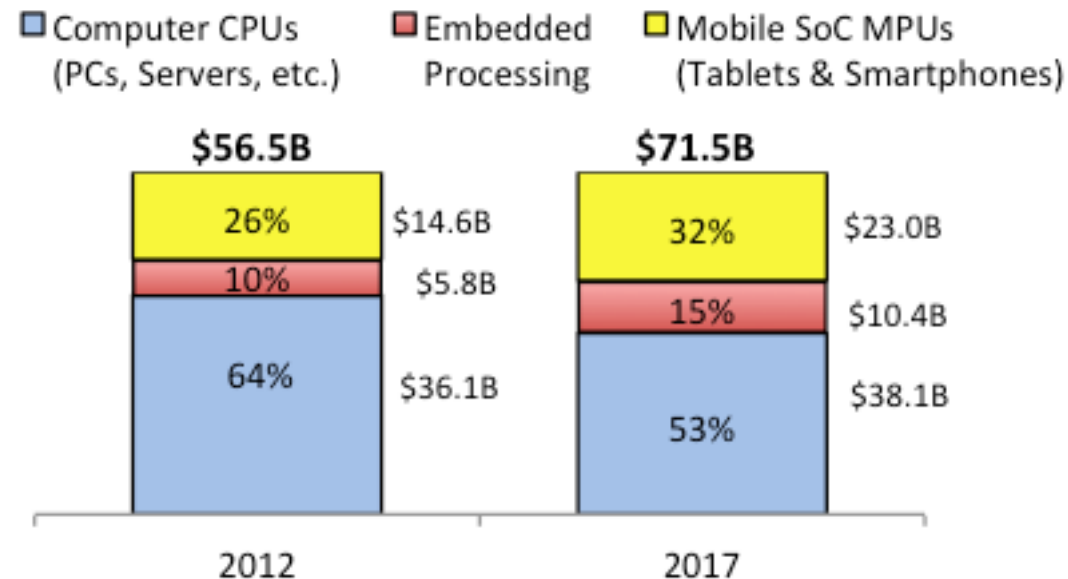
Raspodela na tržištu

2018 MPU Sales by Application (Fcst, \$74.5B)



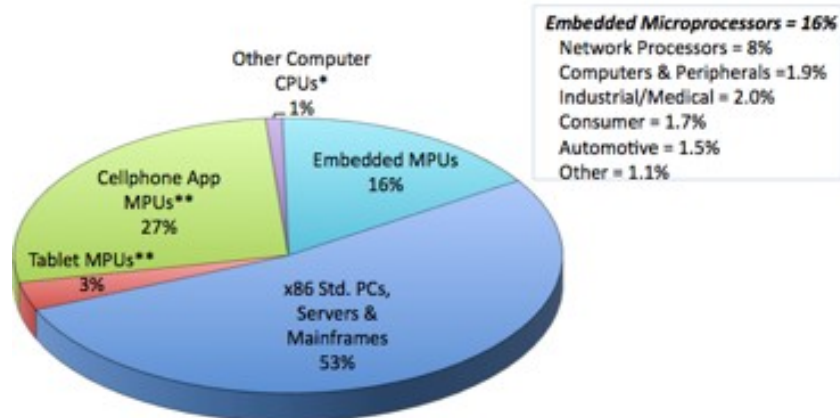
*Includes ARM-based and x86 processors. **Includes ARM-based and other RISC processors.
 Source: IC Insights

Shifting Microprocessor Sales



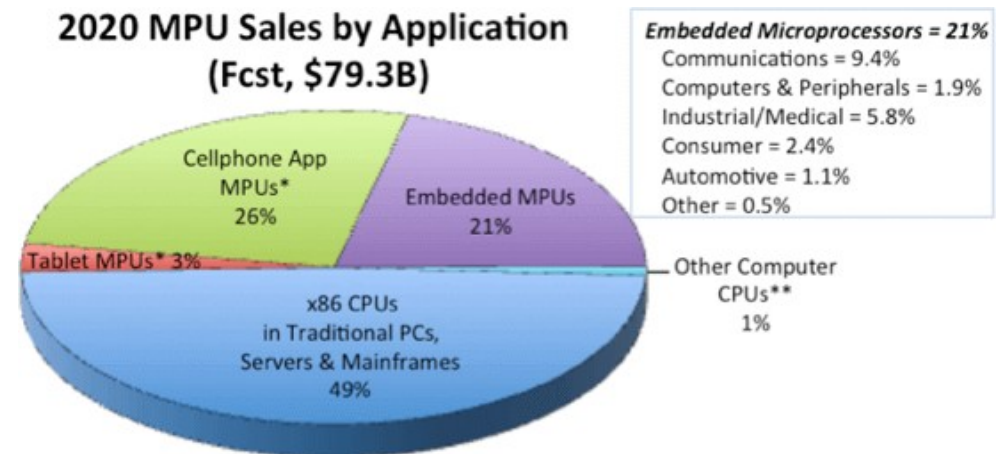
Source: IC Insights

2019 MPU Sales by Applications (Fcst, \$80.3B)



*Covers ARM and other RISC MPUs in servers and workstations.
 **Includes ARM and x86 mobile application processors.
 Source: IC Insights

2020 MPU Sales by Application (Fcst, \$79.3B)

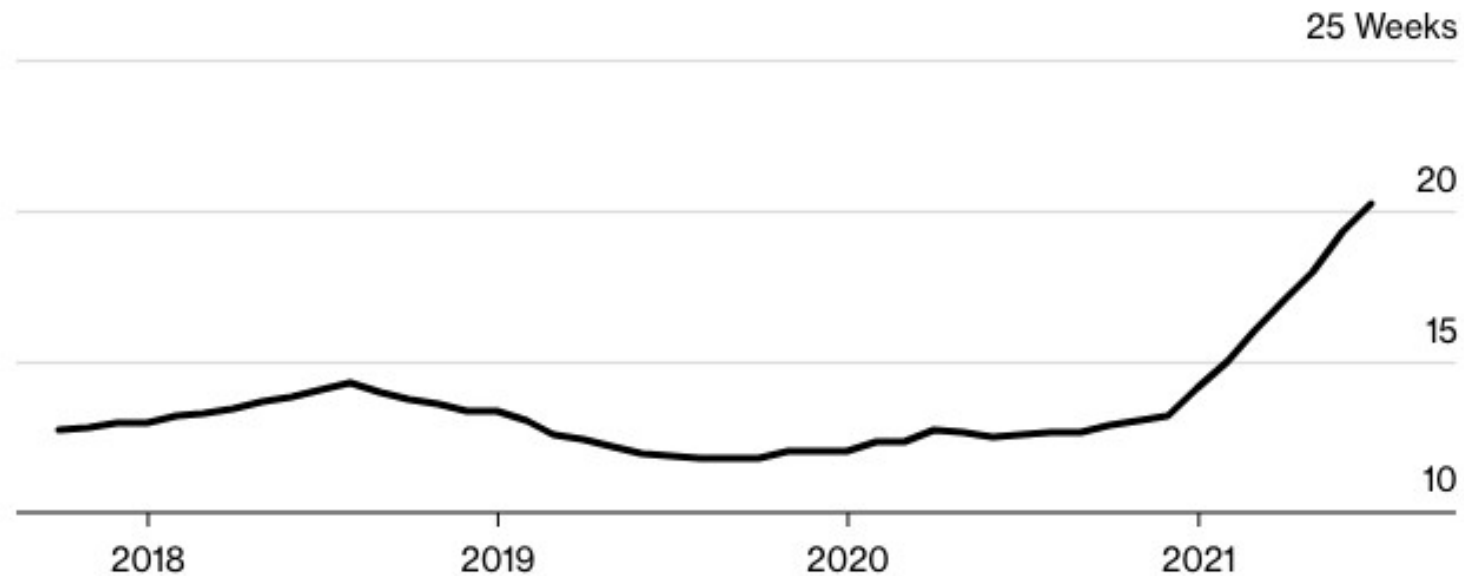


*Includes ARM-based and x86 processors. **Includes ARM-based and other RISC processors.
 Source: IC Insights

Novi problemi

The Long Wait For Chips

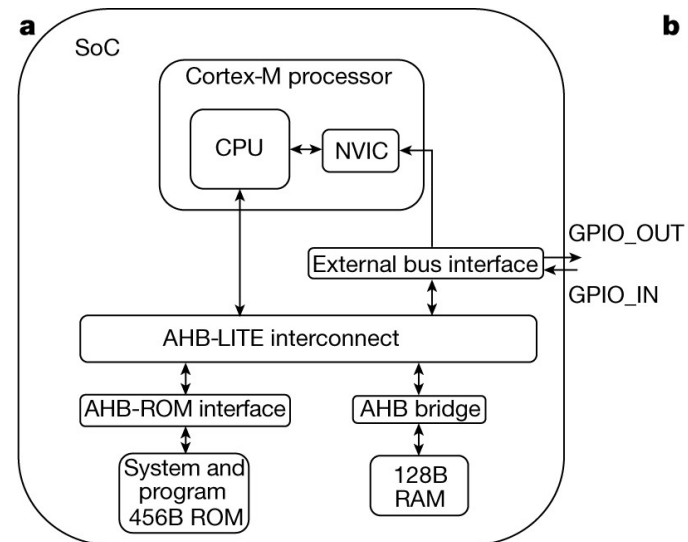
The gap between ordering a chip and delivery is still growing



Source: Susquehanna Financial Group

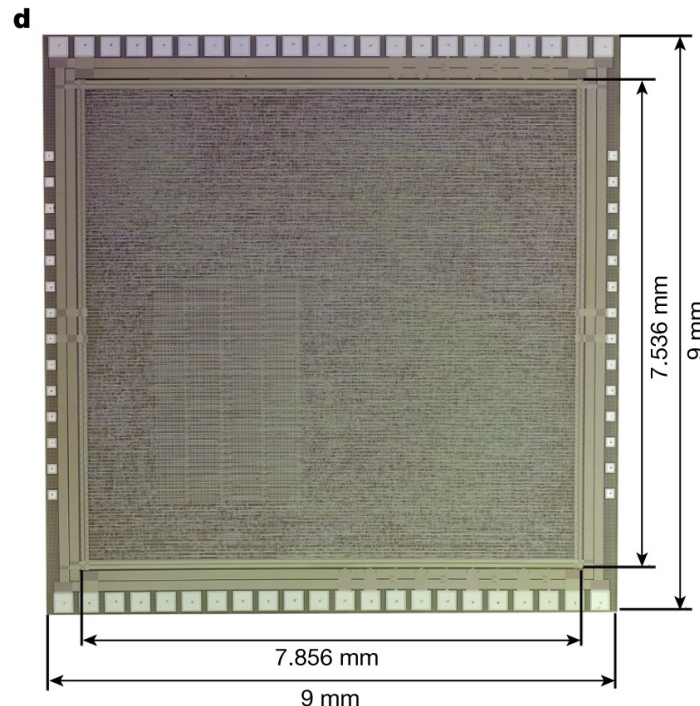
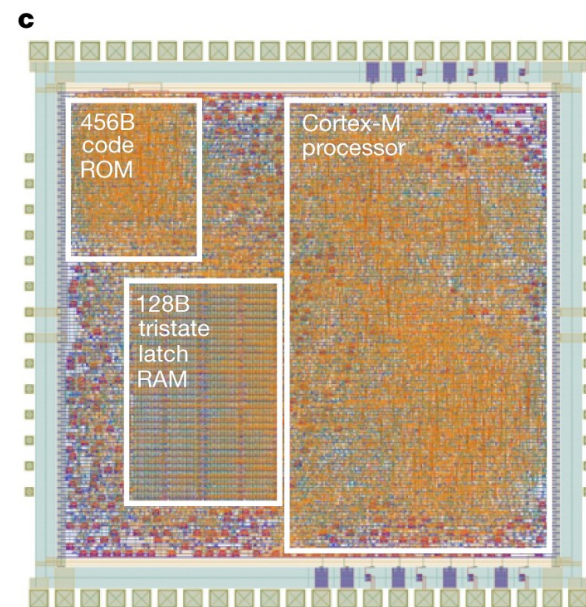
Neka nova rešenja?

Neka nova rešenja?



b

Features	Cortex-M0+ CPU	Cortex-M CPU in PlasticARM
Processor architecture	ARMv6-M	ARMv6-M
Instruction set architecture	16-bit Thumb and a subset of 32-bit Thumb	16-bit Thumb and a subset of 32-bit Thumb
Data and address width	32	32
Number of instructions	86	86
Pipeline	2-stage	2-stage
Architectural register file	Inside the CPU	Mapped to RAM external to the CPU
Binary compatibility	Can run code from other Cortex-M CPUs	Can run code from other Cortex-M CPUs including Cortex-M0+



-prvi fleksibilni
32-bitni ARM [5]

[5] J. Biggs, J. Myers, J. Kufel et al. A natively exible 32-bit Arm microprocessor, Nature 595, pp. 532-536, 2021.

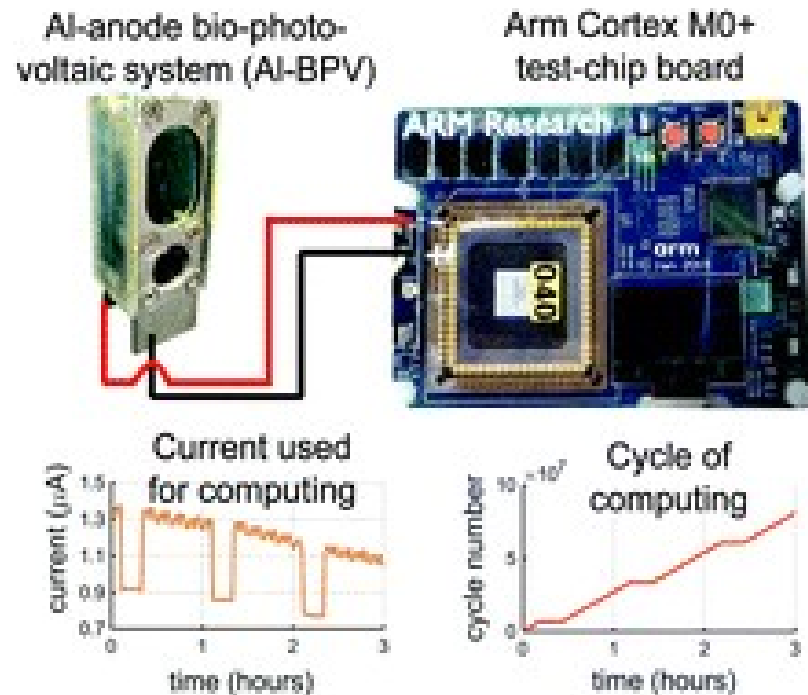
PlasticARM

Feature	PlasticARM (this work)	Flexible 8-bit ALU ¹⁶	Dedicated machine learning FlexIC ⁷	BNN FlexIC ¹⁸
Area (mm ²)	59.2	225.6	5.6	5.86
Technology	0.8-μm metal-oxide TFT	5-μm dual-gate organic + metal-oxide TFTs	0.8-μm metal-oxide TFT	0.8-μm metal-oxide TFT
Logic type	Unipolar n-type resistive load	Complementary n-type oxide and p-type organic	Unipolar n-type resistive load	Unipolar n-type resistive load
Supply voltage (V)	3	6.5	4.5	3
Chip pin count	28	30	23	23
Processor	32-bit Arm Cortex-M-based SoC	8-bit ALU + P ² ROM	Custom hardware	Custom hardware
Number of devices	56,340 (39,157 TFTs plus 17,183 resistors)	3,504	3,132 (2,084 TFTs + 1,048 resistors)	4,489 (3,028 TFTs + 1,461 resistors)
NAND2-equivalent gate count	18,334	876	1,024	1,421
Max circuit clock frequency (kHz)	29	2.1	104	22
Power consumption (mW)	21	Not reported	7.2	1.1
Power density (mW mm ⁻²)	0.4	Not reported	1.3	0.2

J. Biggs, J. Myers, J. Kufel et al. A natively exible 32-bit Arm microprocessor, Nature 595, pp. 532-536, 2021.

Neka nova rešenja?

- Univerzalna memorija [6] ?
(UltraRAM)
- Serverless computing, the container era, IaaS, HaaS
- Blockchain
- Baterija od algi



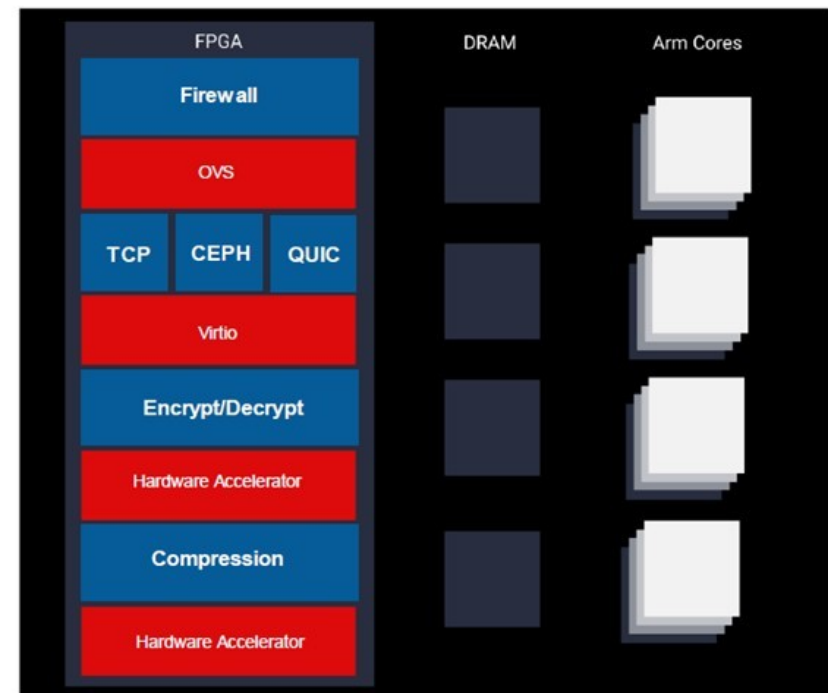
[6] D. Lane and M. Hayne, "Simulations of Ultralow-Power Nonvolatile Cells for Random-Access Memory," in *IEEE Transactions on Electron Devices*, vol. 67, no. 2, pp. 474-480, Feb. 2020, doi: 10.1109/TED.2019.2957037.

- Xilinx Alveo

Introducing The Xilinx Alveo SN1000

- ▶ **Software-defined hardware acceleration**
- ▶ Application specific data paths
- ▶ Build **custom offloads** or **extend existing offloads** to handle new protocols and applications

Example 1



Alveo U25N

The Alveo U25N SmartNIC delivers a true convergence of network and security acceleration functions, including OVS and IPsec, into a single platform.

[Learn More >](#)



Alveo U30

The Alveo U30 media accelerator card provides low latency video processing (32ms for 4Kp60) for live streaming, supporting mainstream H.264 and H.265 standards and also available on the AWS cloud for evaluation or deployment.

[Learn More >](#)



Alveo MA35D

The Alveo MA35D delivers ultra-low latency (8ms for 4Kp60) video processing for live streaming, supporting the next-generation AV1 codec standard and mainstream H.264 and H.265 formats.

[Learn More >](#)



Alveo U45N

The 2x 100G Alveo U45N network accelerator offloads server CPUs from infrastructure workloads in the data center. FPGA designers can implement custom OVS, IPsec, and other functions with the ability to adapt to evolving use cases.

[Learn More >](#)



Alveo U50

Delivers compute, networking, and storage acceleration in an efficient 75-watt, small form factor, and armed with 100 GbE networking, PCIe Gen4, and HBM2. Designed to deploy in any server.

[Learn More >](#)



Alveo U55C

Built for HPC and Big Data applications, the Alveo U55C accelerator is the most powerful Alveo card ever from AMD.

[Learn More >](#)



Overview

Acceleration for Dynamic Workloads



Fast
Highest Performance



Adaptable
Accelerate Any Workload

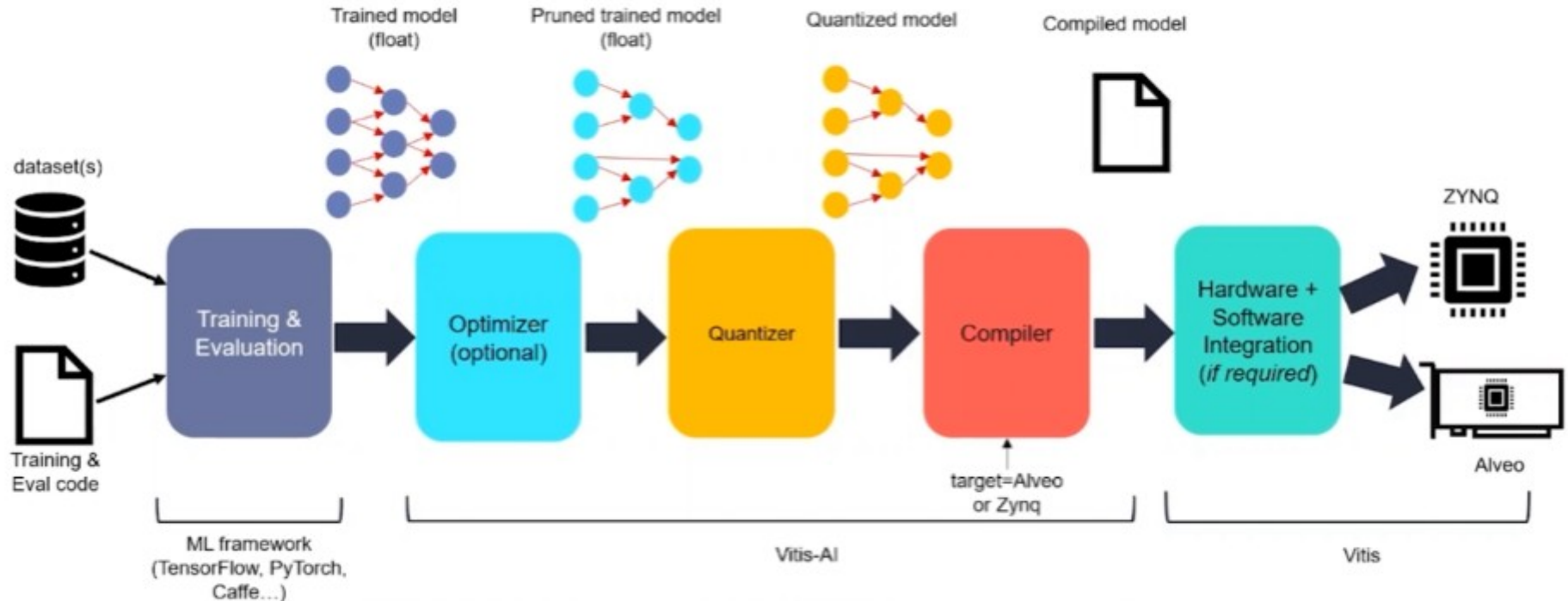


Accessible
Cloud ↔ On-Premises Mobility



- Xilinx Automotive

Unified Edge/Cloud Development Flow



HVALA NA PAŽNJI!

