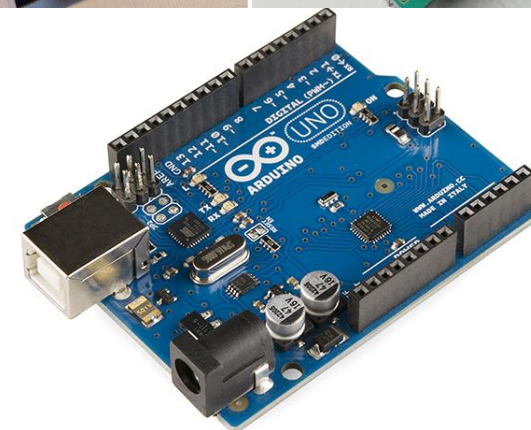
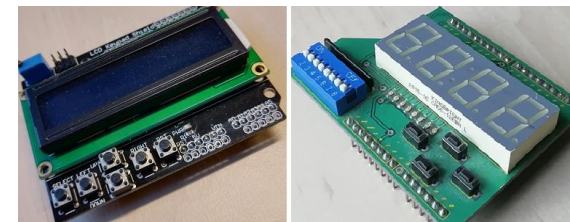
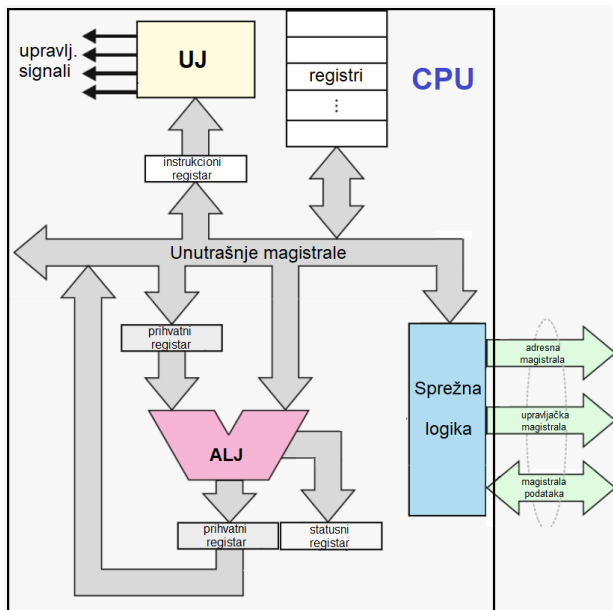
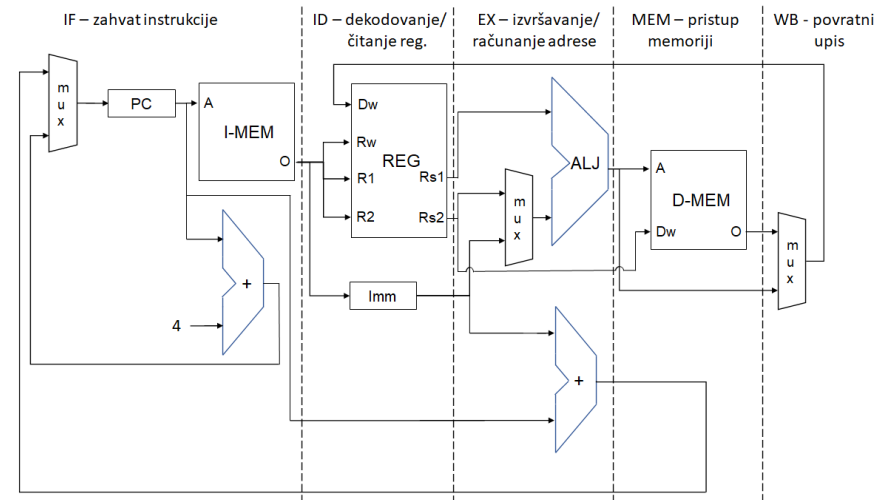
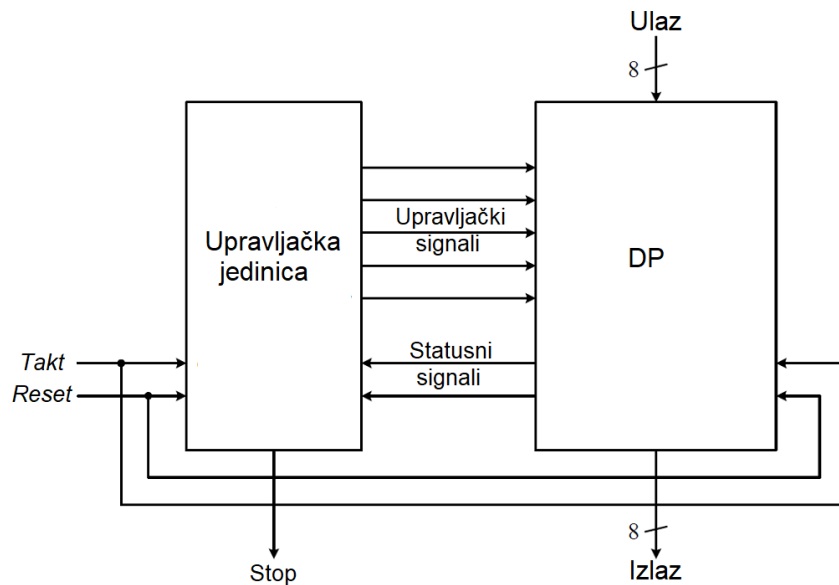


# Osnovi mikroprocesorskih i mikrokontrolerskih sistema



**Uvodno predavanje**  
prof. dr Ivan Mezei

## **Nastavnik**

dr Ivan Mezei, red. prof.

Kabinet: NTP-135

telefon: 485 4519

email: imezei@uns.ac.rs

Konsultacije: po dogovoru

## **Asistenti**

MSc Anja Tanović

BSc Stojanka Bratić

BSc David Vidović

## **Demonstratori**

# Malo istorije

- od 1999-2022. g. Mikroprocesorska elektronika (3. god.)
- assembler za x86 u prvom semestru
- assembler za x51 u drugom semestru
  
- kasnije je predmet postao jednosemestralni (V semestar) i oblikovan da se radi samo u vezi x51
  
- danas je ideja predmeta da osposobi studente za osnovni rad sa mikroprocesorima i mikrokontrolerima

## Okvirni sadržaj predavanja:

Uvodno predavanje

Osnovi arhitektura mikrokontrolera i mikroprocesora

Različite arhitekture i podsistemi mikroprocesora

Principi projektovanja mikroprocesora

Primeri projektovanja jednostavnijih procesora (mCPU0, mCPU1, mEdulent, itd.)

Memorijski podsystem

Uvod u RISC mikroprocesore

## K1

Arhitektura, organizacija memorije i skup instrukcija mikrokontrolera ATmega328p

Rad sa periferijama

Prekidi

Tajmeri i brojači

Serijska komunikacija

## K2

## Sadržaj lab. vežbi:

1. nedelja - nema
2. 3. i 4. nedelja - Uvod u školski mikroračunar Edulent, rad sa simulatorom školskog mikroračunara Edulent i programiranje u simboličkom mašinskom jeziku za Edulent
5. nedelja – LK1
6. 7. i 8. nedelja - Uputstvo i jezičke reference za Arduino razvojni sistem, LCD displej + tastatura
9. i 10. nedelja - 4x7SEG displej + LED diode + tasteri + prekidači
11. i 12. nedelja - Tajmeri i prekidi
13. nedelja – LK2

Cilj predmeta je da studente osposobi za razumevanje svih funkcionalnih blokova savremenih mikroprocesora i mikrokontrolera.

Cilj je i osposobiti studente za projektovanje, pisanje i testiranje aplikativnih i sistemskih programa za projektovane mikroračunarske sisteme.

Student koji uspešno završi ovaj predmet biće u stanju da:

- razume rad, modeluje i projektuje na strukturalnom nivou, mikroračunarske sisteme zasnovane na mikroprocesorima i mikrokontrolerima na osnovu zadate specifikacije;
- modeluje, projektuje, simulira i implementira jednostavne aplikativne i systemske programe u simboličkom mašinskom jeziku i programskom jeziku visokog nivoa za zadati mikroračunarski sistem; i
- testira mikroračunarski sistem na razvojnom sistemu.

## Materijali na sajtu i knjiga:

1006

UNIVERZITET U NOVOM SADU  
FAKULTET TEHNIČKIH NAUKA  
EDICIJA TEHNIČKE NAUKE - UDŽBENICI



1006

Ivan Mezei OSNOVI MIKROPROCESORSKIH I MIKROKONTROLERSKIH SISTEMA

Ivan Mezei

### OSNOVI MIKROPROCESORSKIH I MIKROKONTROLERSKIH SISTEMA

Novi Sad, FTN 2022



**Teorija:** 50%

**Vežbe:** 50%

**Aktivnost:** do 5%

Plan:

- Kolokvijum LK1 u labu iz vežbi - Edulent 20% (u toku 5. nedelje počevši od 18.03.)
- Kolokvijum K1 u učionici nakon 1. dela teorije 25% (22.04.)
- Kolokvijum LK2 u labu iz Arduina 30% pred kraj semestra
- Kolokvijum K2 nakon 2. dela teorije 25% u poslednjoj nedelji (10.06.)

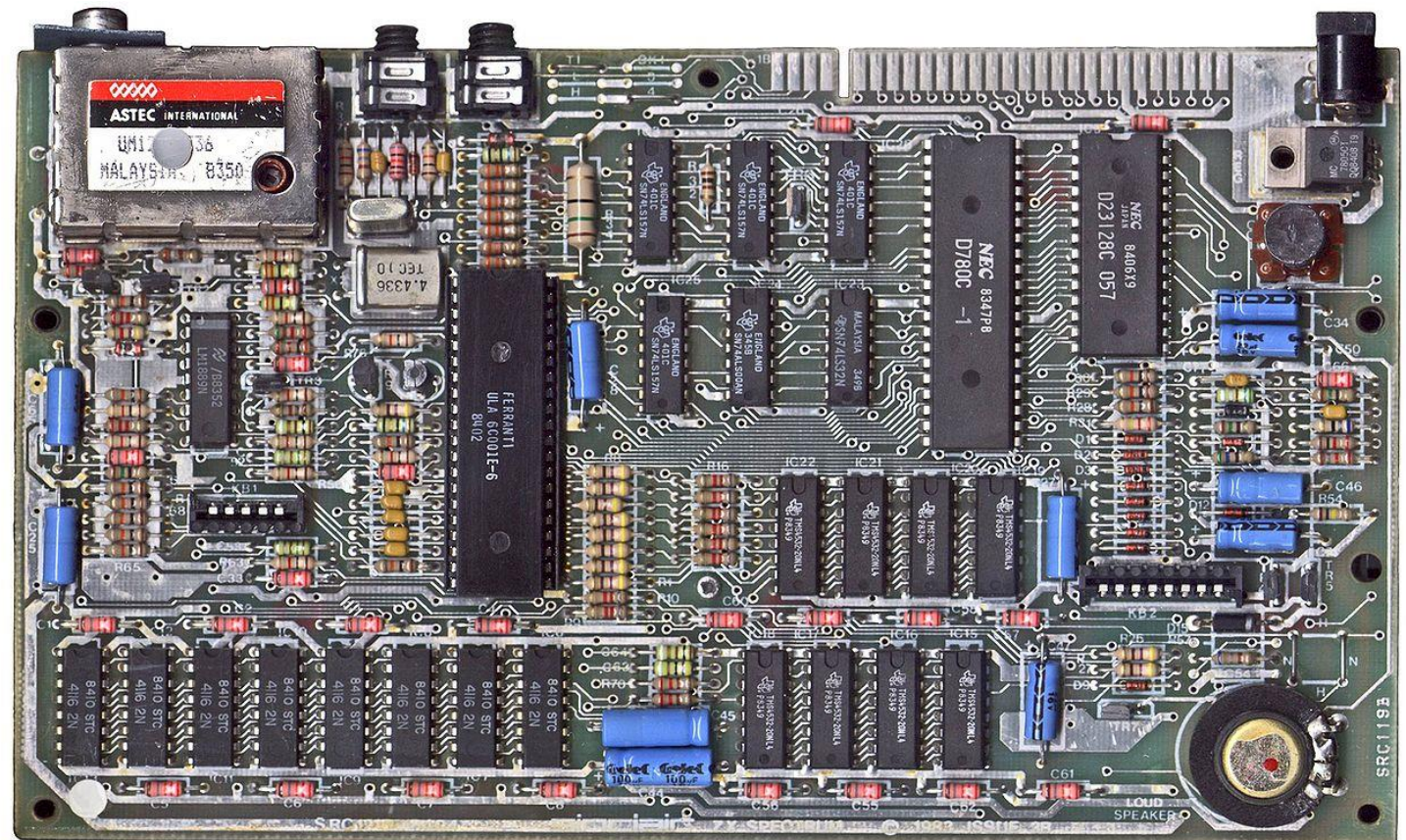
## **NAPOMENA:**

Da bi se teorija i vežbe računale kao urađene potrebno je da imate barem oko pola poena iz zbirno K1+K2 i isto iz LK1+LK2!

# Proizvodnja mikroprocesora



# Proizvodnja mikroprocesora





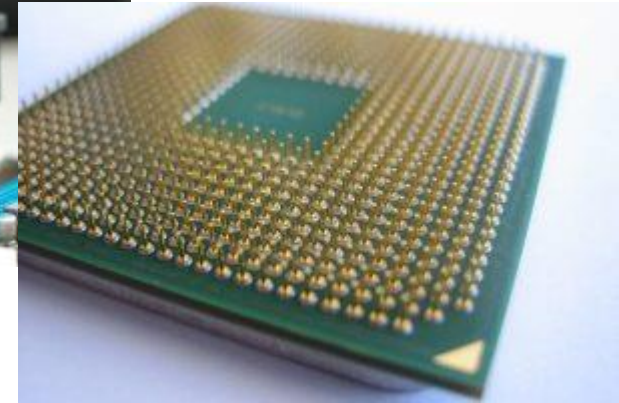
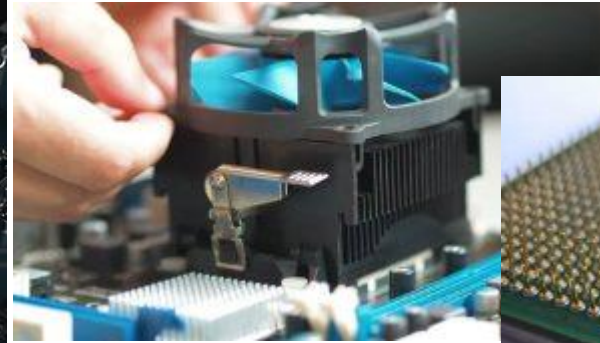
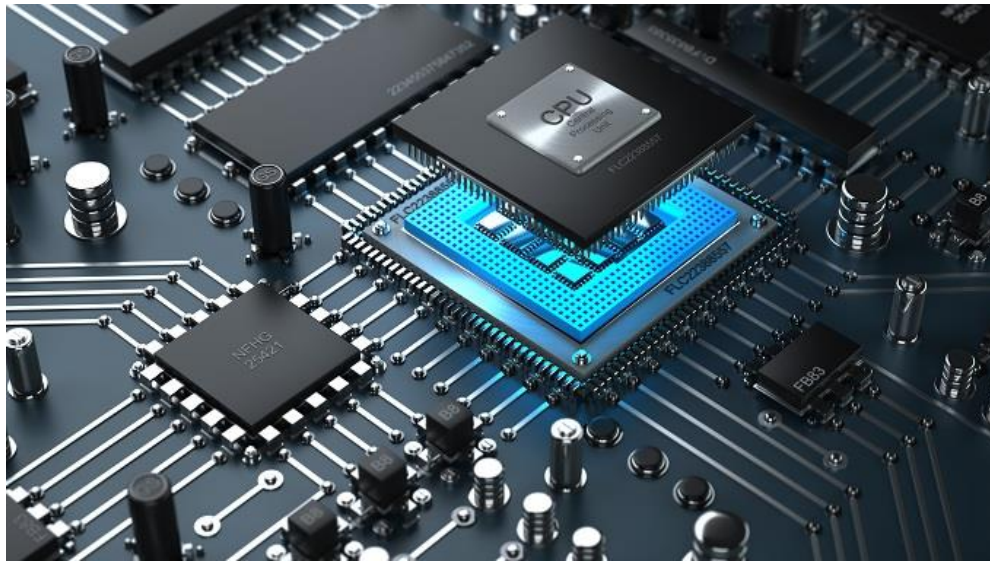
## 90' Era personalnih računara



# Intel pentium 1,2,3,4



# Poslednjih 10tak godina

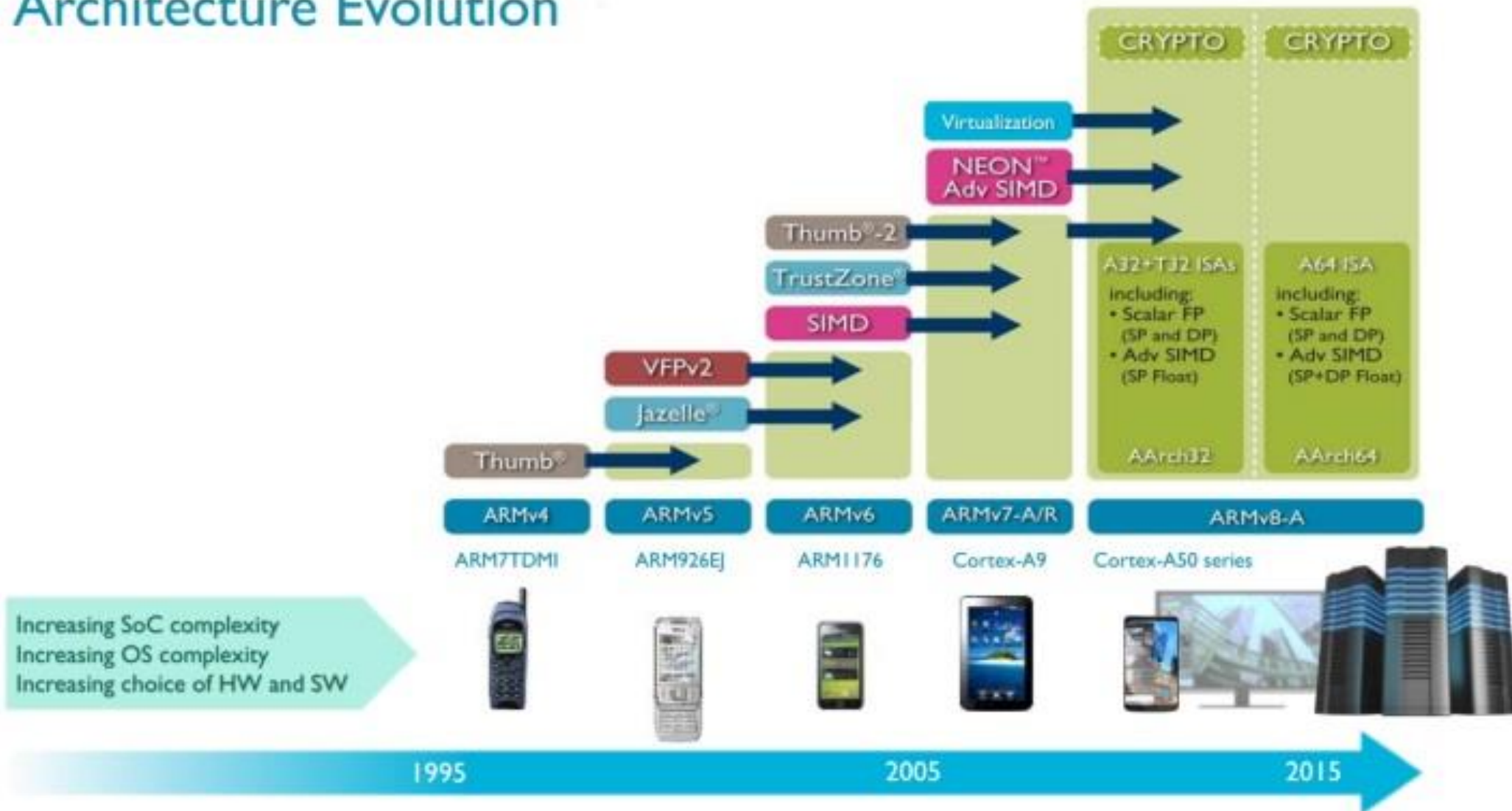


intel  
14<sup>th</sup> Gen  
Core





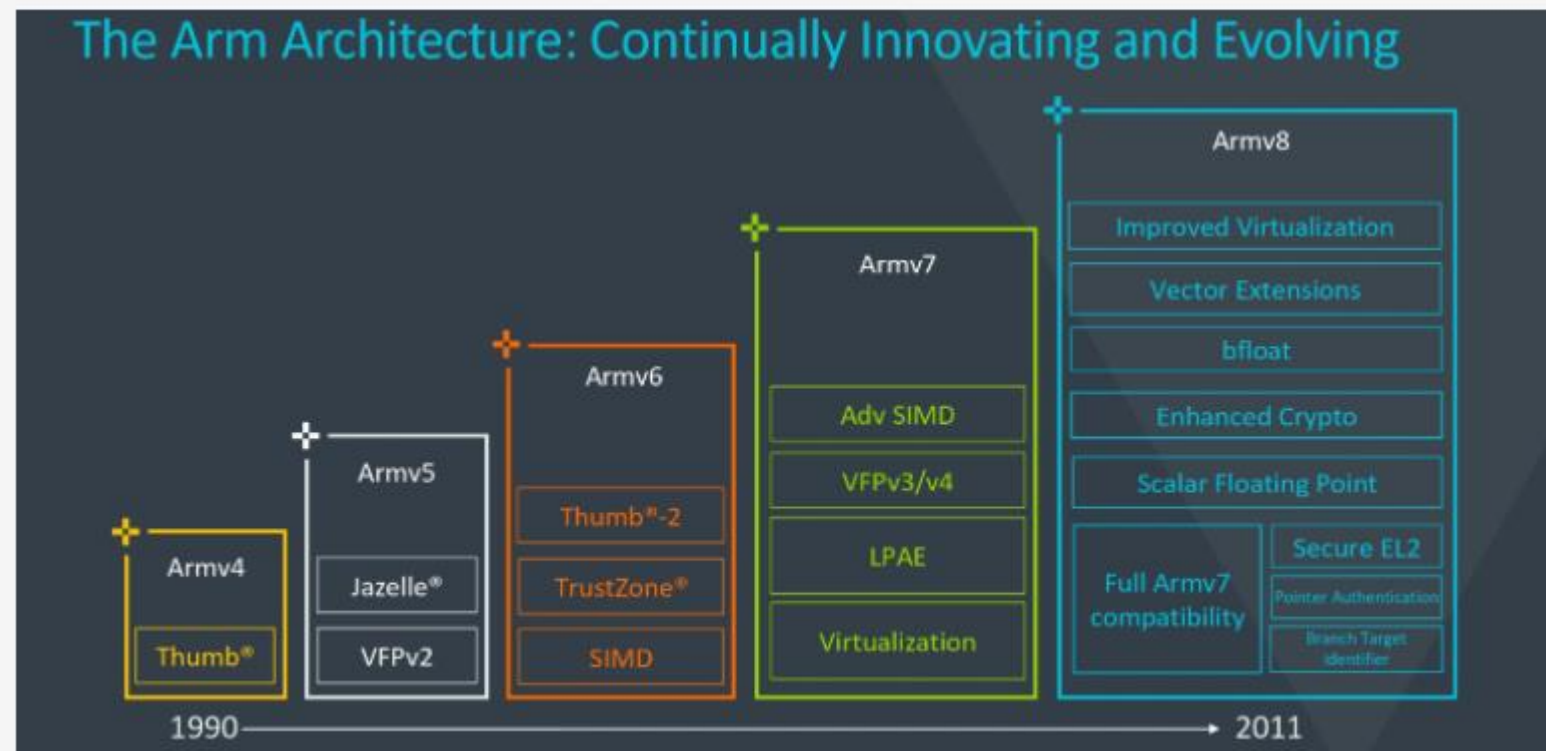
## Architecture Evolution



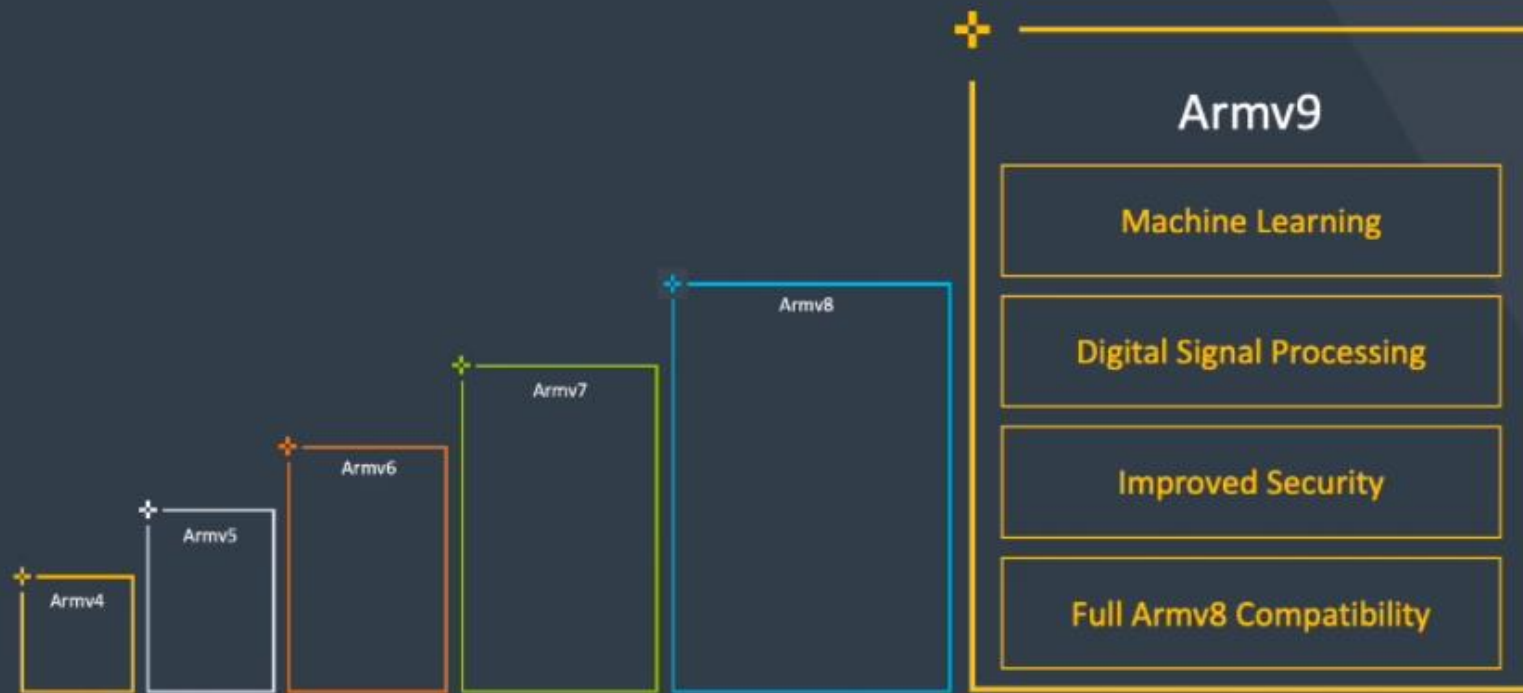
## Arm Launches ARMv9

March 30, 2021 David Schor ARM, ARMv8, ARMv9, Confidential Compute Architecture (CCA), Scalable Vector Extension (SVE), Scalable Vector Extension 2 (SVE2)

Ten years ago Arm launched a new 64-bit architecture. ARMv8 more than just extended the virtual address space over ARMv7. It cleaned up and streamlined the architecture and eliminated legacy quirks. ARMv8 has proven to be an extremely successful architecture, adding numerous new features over the next decade. Today, Arm is launching its successor – ARMv9 for the next decade.



## Introducing Armv9: The Secure Architecture for All Workloads

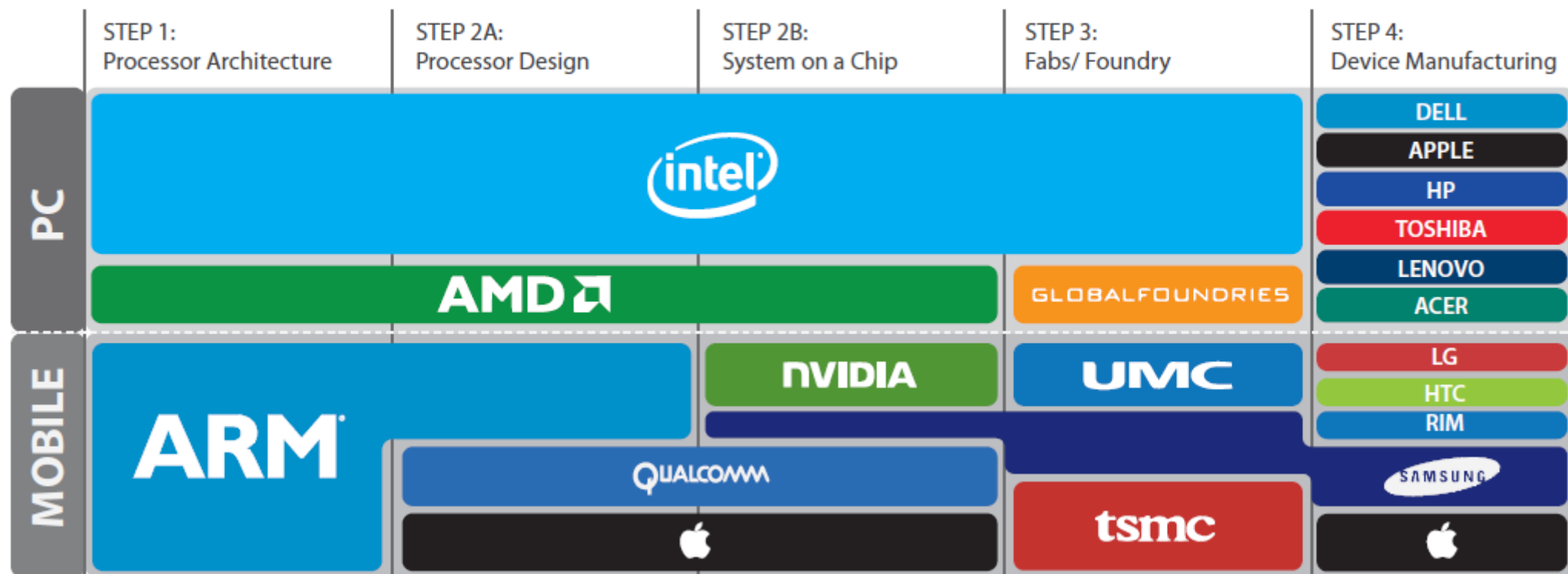


**Powering the next  
300 billion chips**



# Proizvodnja procesora

## Processor Value Chain



# Novost (ali ipak odustali)



## NEWSROOM

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### Press Release

## NVIDIA to Acquire Arm for \$40 Billion, Creating World's Premier Computing Company for the Age of AI

Sunday, September 13, 2020



## Intel & Arm Product

### INTEL

- High End Powerful MicroProcessors
- Broad Product Range

Commonly Found in...



### ARM

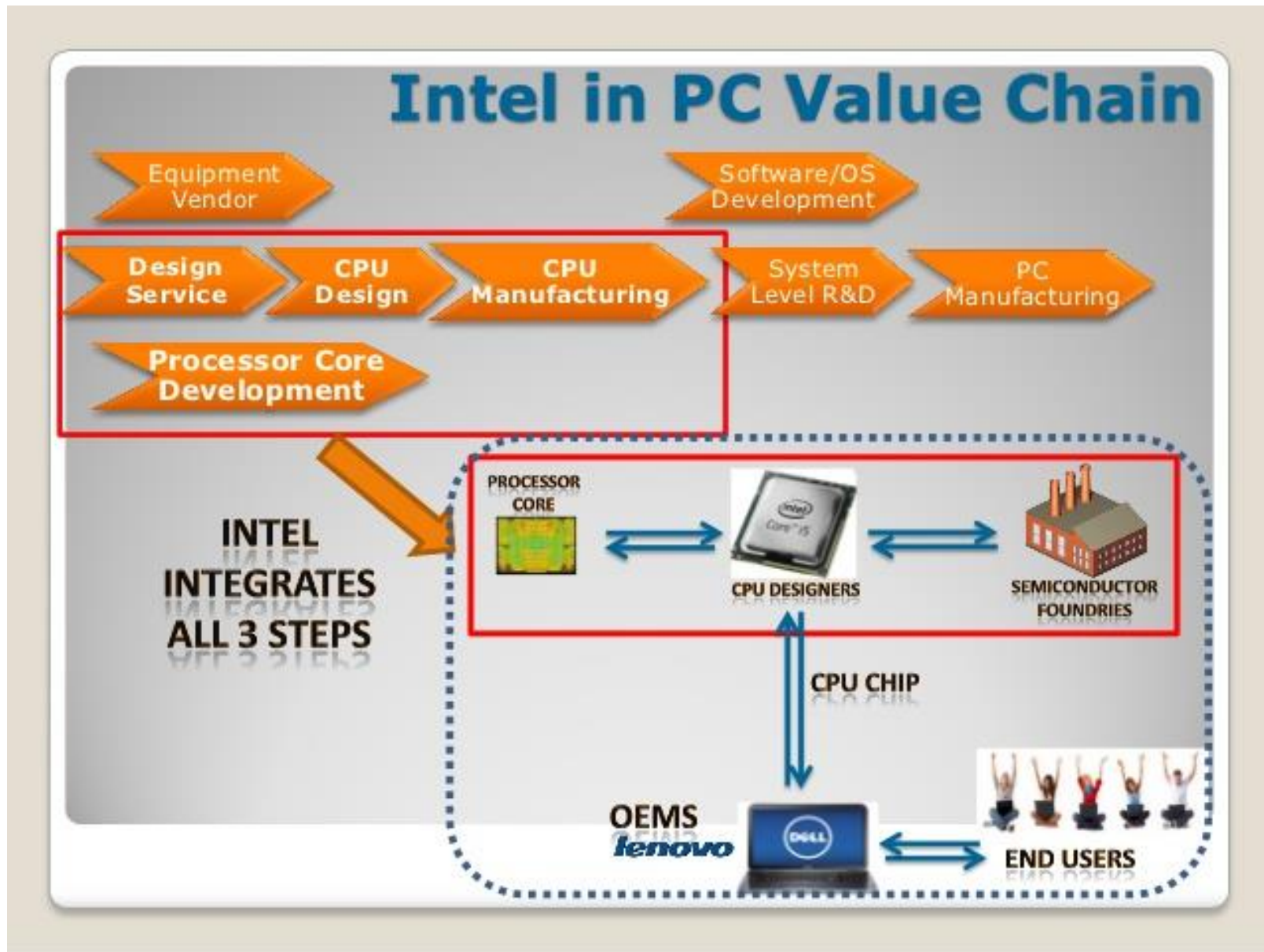
- Mobile Chips
- Small and Light
- Low Energy Consumption

Commonly Found in...



## ARM

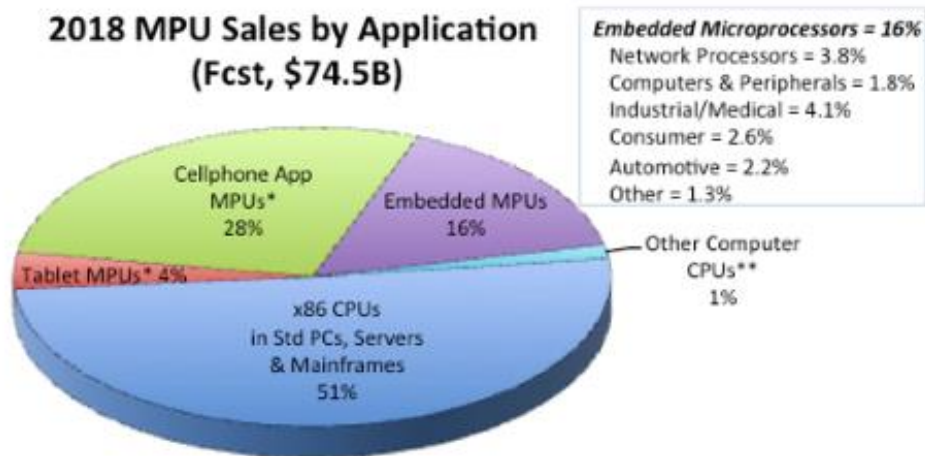






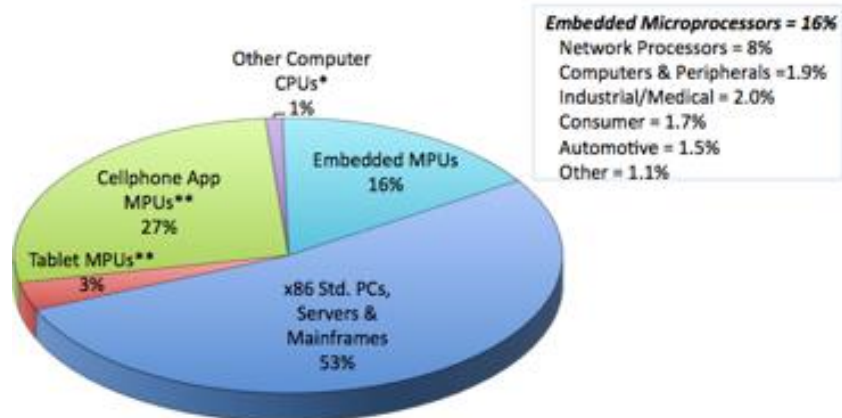
# Raspodela na tržištu

**2018 MPU Sales by Application (Fcst, \$74.5B)**



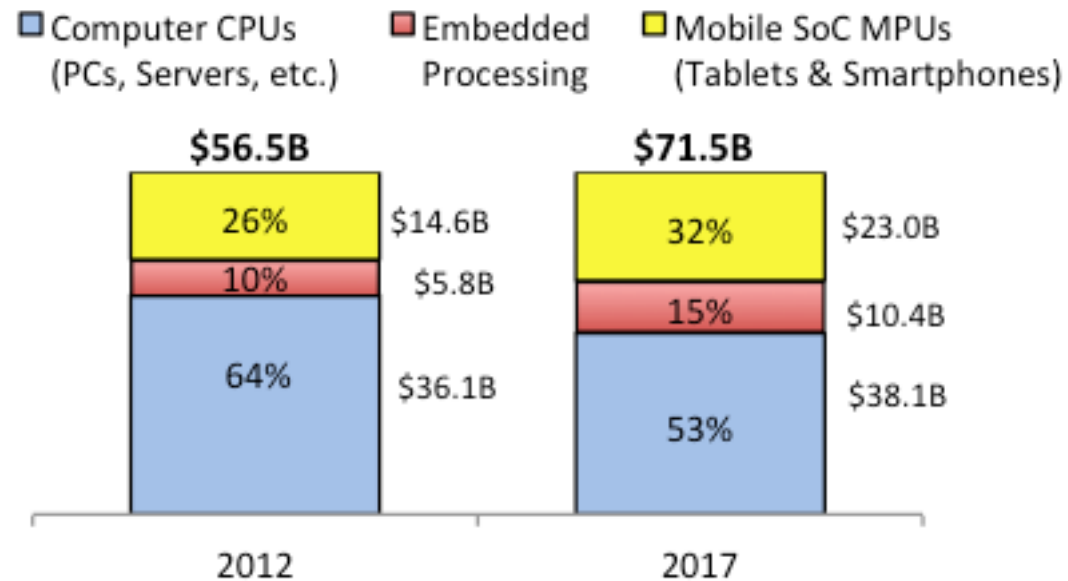
\*Includes ARM-based and x86 processors. \*\*Includes ARM-based and other RISC processors.  
 Source: IC Insights

**2019 MPU Sales by Applications (Fcst, \$80.3B)**



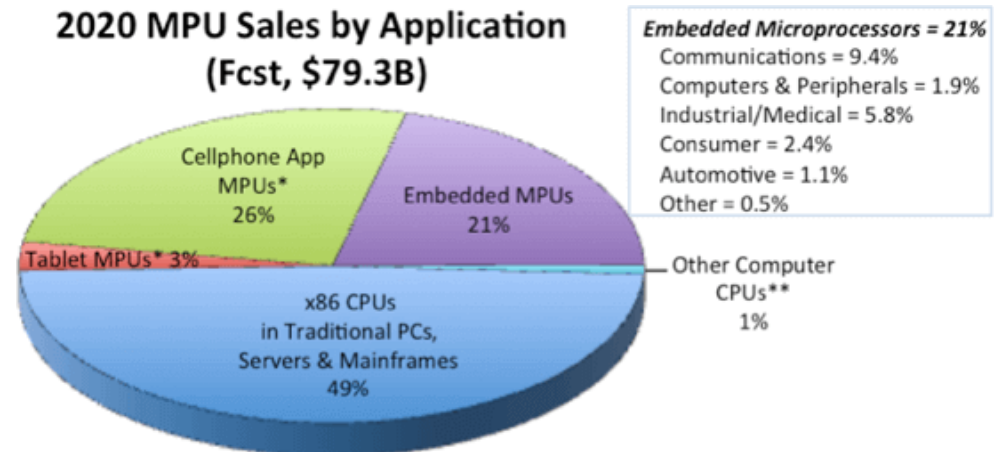
\*Covers ARM and other RISC MPUs in servers and workstations.  
 \*\*Includes ARM and x86 mobile application processors.  
 Source: IC Insights

## Shifting Microprocessor Sales



Source: IC Insights

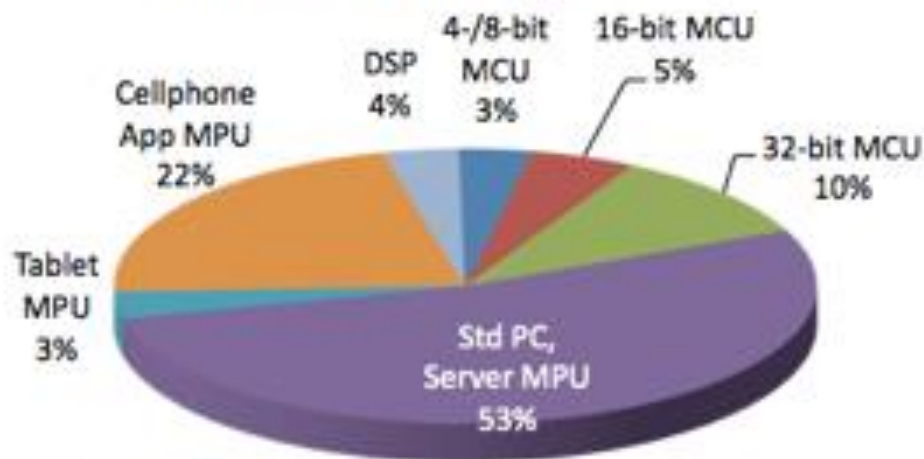
**2020 MPU Sales by Application (Fcst, \$79.3B)**



\*Includes ARM-based and x86 processors. \*\*Includes ARM-based and other RISC processors.  
 Source: IC Insights

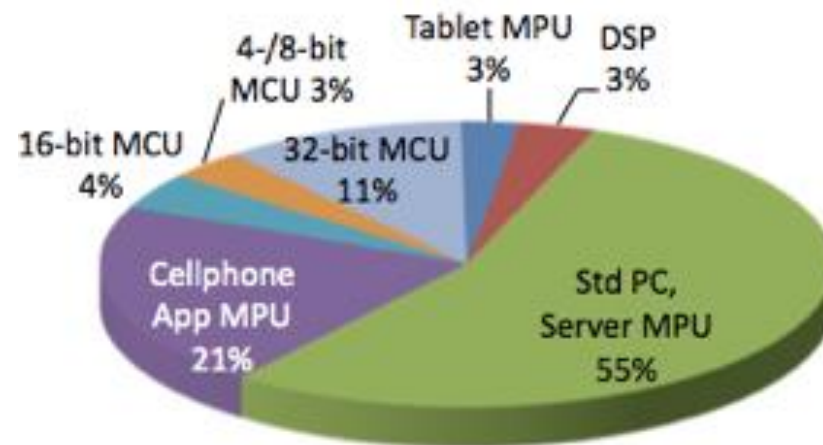
# Raspodela na tržištu

**2018F MOS Microcomponent  
Marketshare (\$95.7B)**



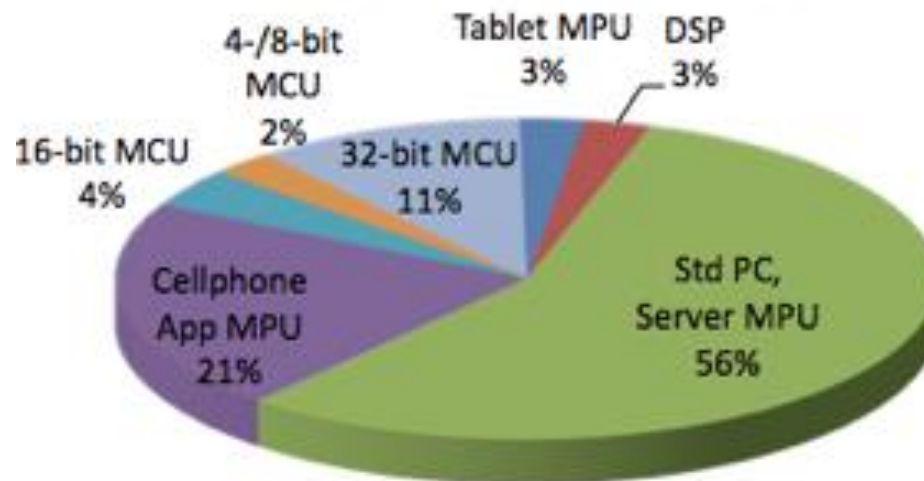
Source: IC Insights

**2019F MOS Microcomponent  
Marketshare (\$102.3B)**



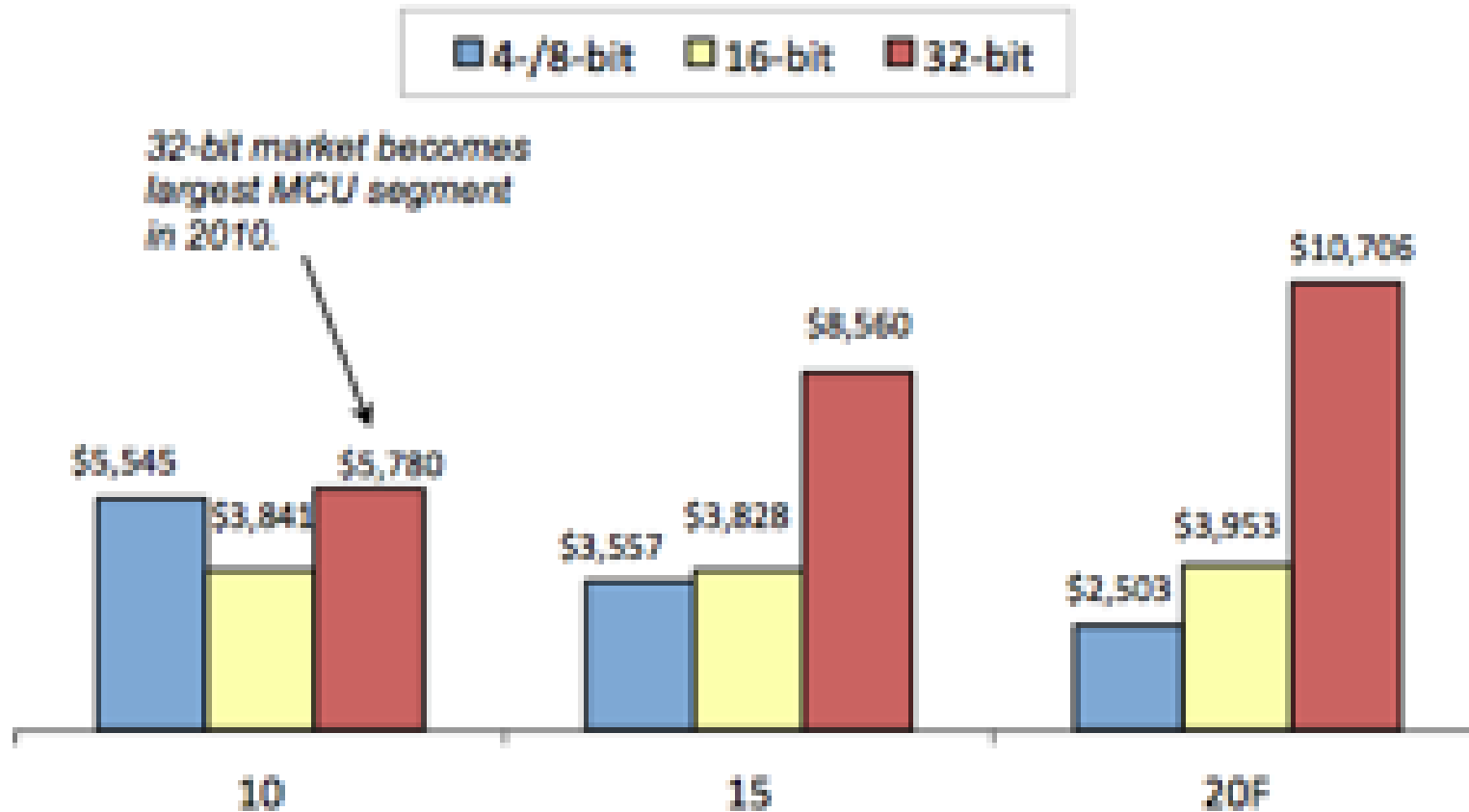
Source: IC Insights

**2020F MOS Microcomponent  
Marketshare (\$100.4B)**



Source: IC Insights

## Shifts in MCU Market (\$M)

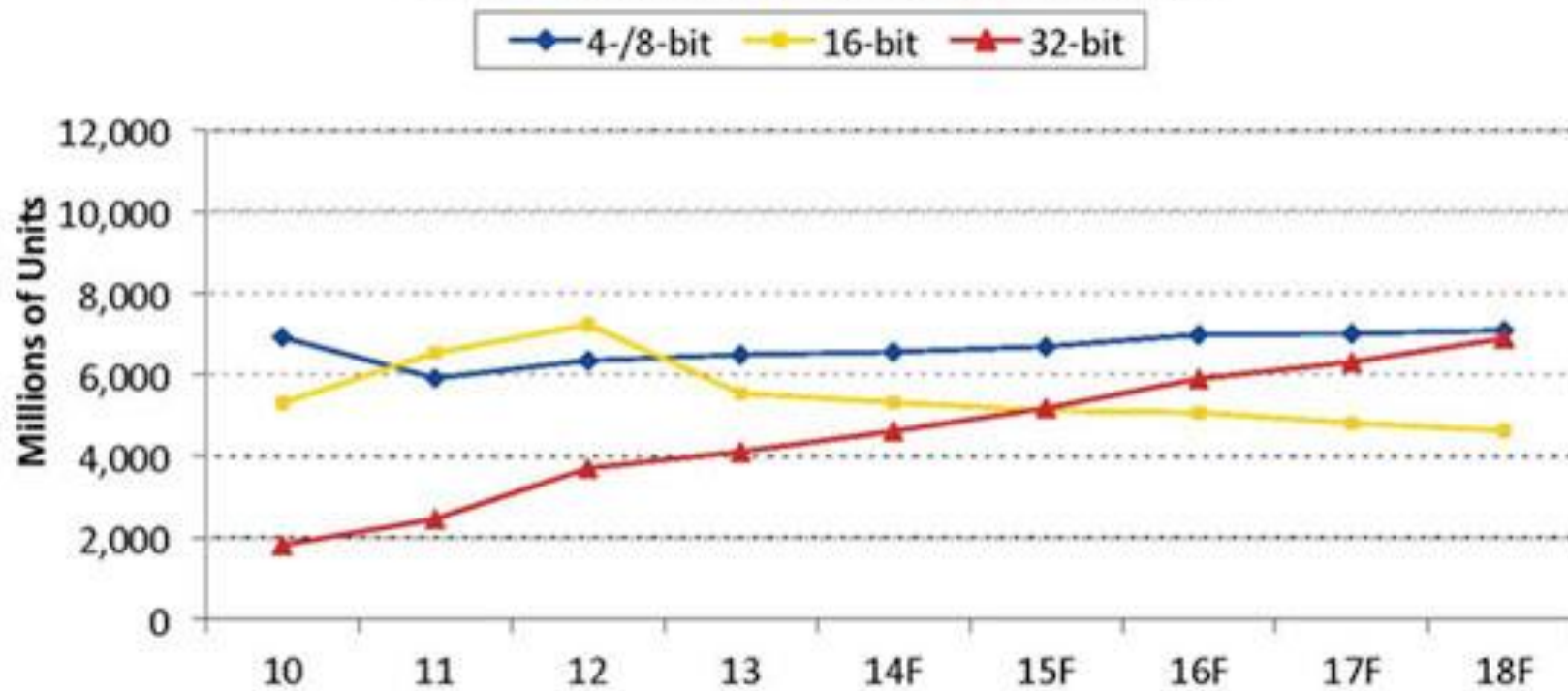


Source: IC Insights



# Prodaja MCU

## MCU Unit Shipments by Category



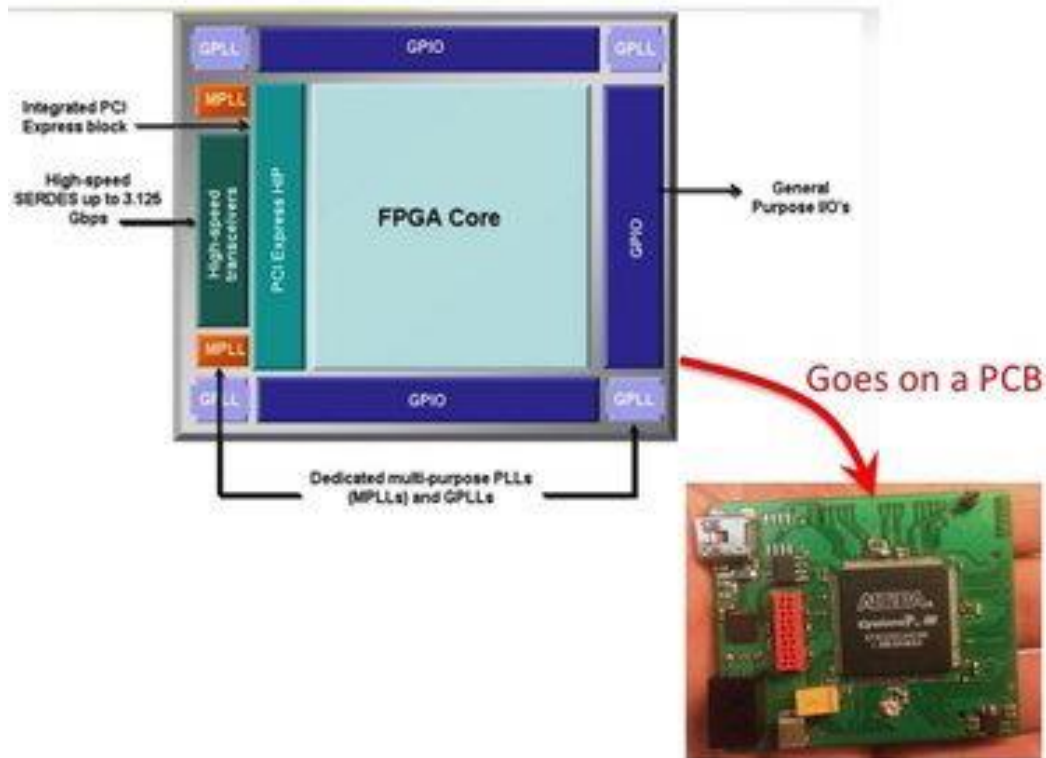
Source: IC Insights' 2014 McClean Report

# Zarada u M\$

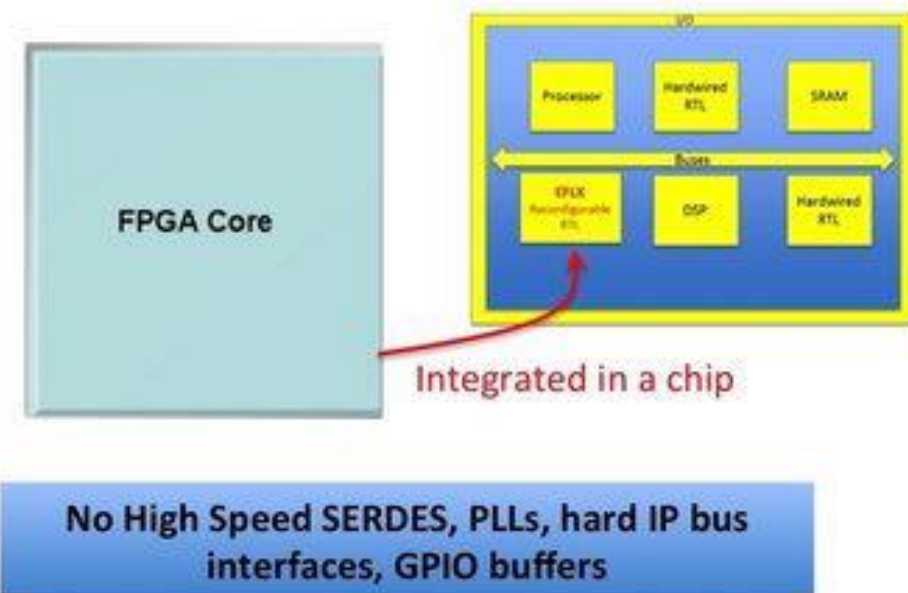
	2012	2013	2014	2015	2016	2017	CAGR
Total Semiconductor	325,367	339,666	361,612	385,052	395,974	413,602	4.9%
Microcontroller (MCU)	16,008	16,202	17,211	18,799	19,307	20,480	5.1%
4 bit MCU	154	159	161	157	145	133	-2.8%
8 bit MCU	6,057	6,565	6,936	7,532	7,768	8,259	6.4%
16 bit MCU	4,021	3,611	3,765	4,060	4,053	4,019	0.0%
32 bit MCU	5,776	5,868	6,349	7,050	7,341	8,069	6.9%

# eFPGA

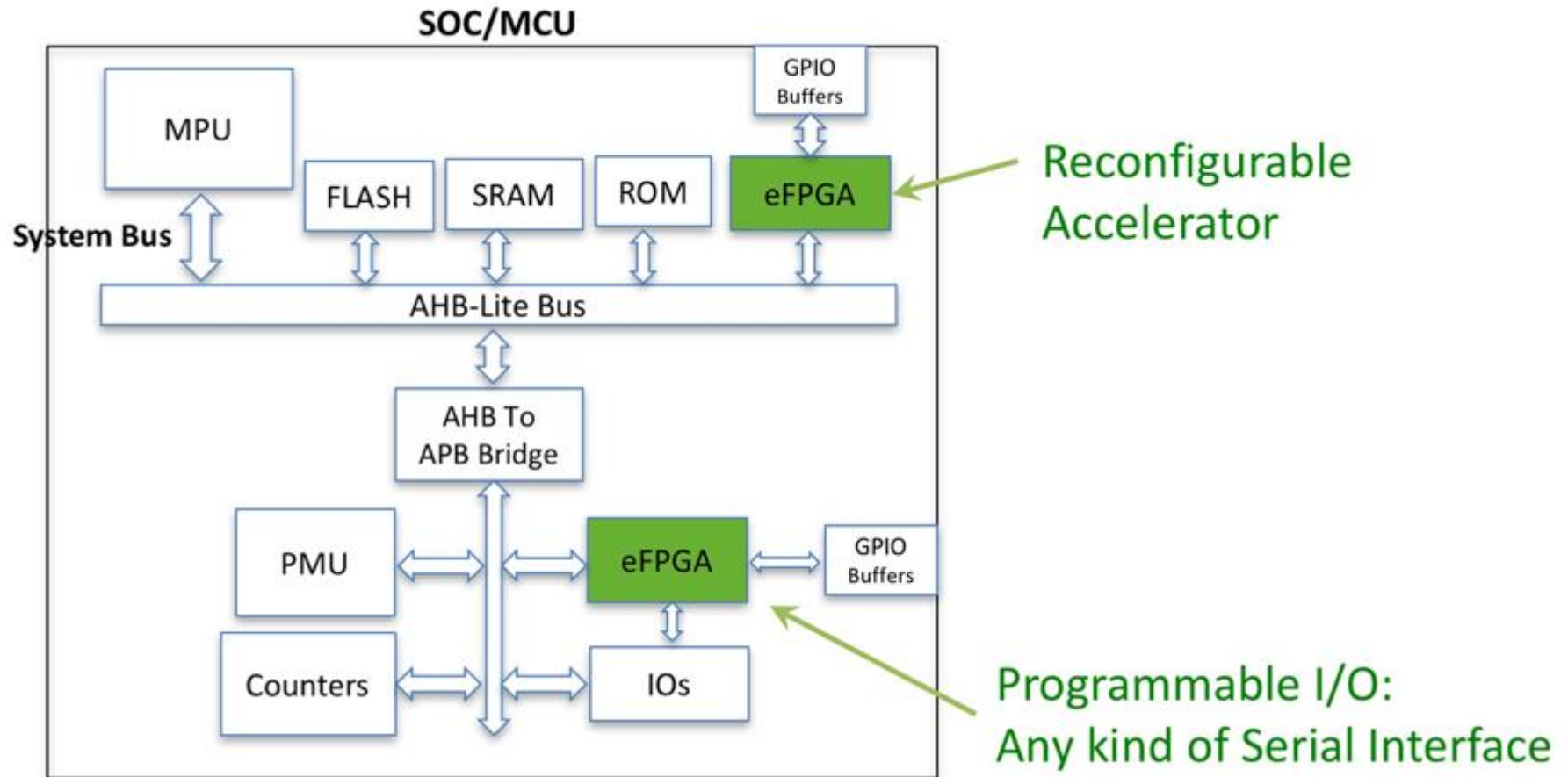
Typical FPGA Chip  
(Altera Cyclone IV)



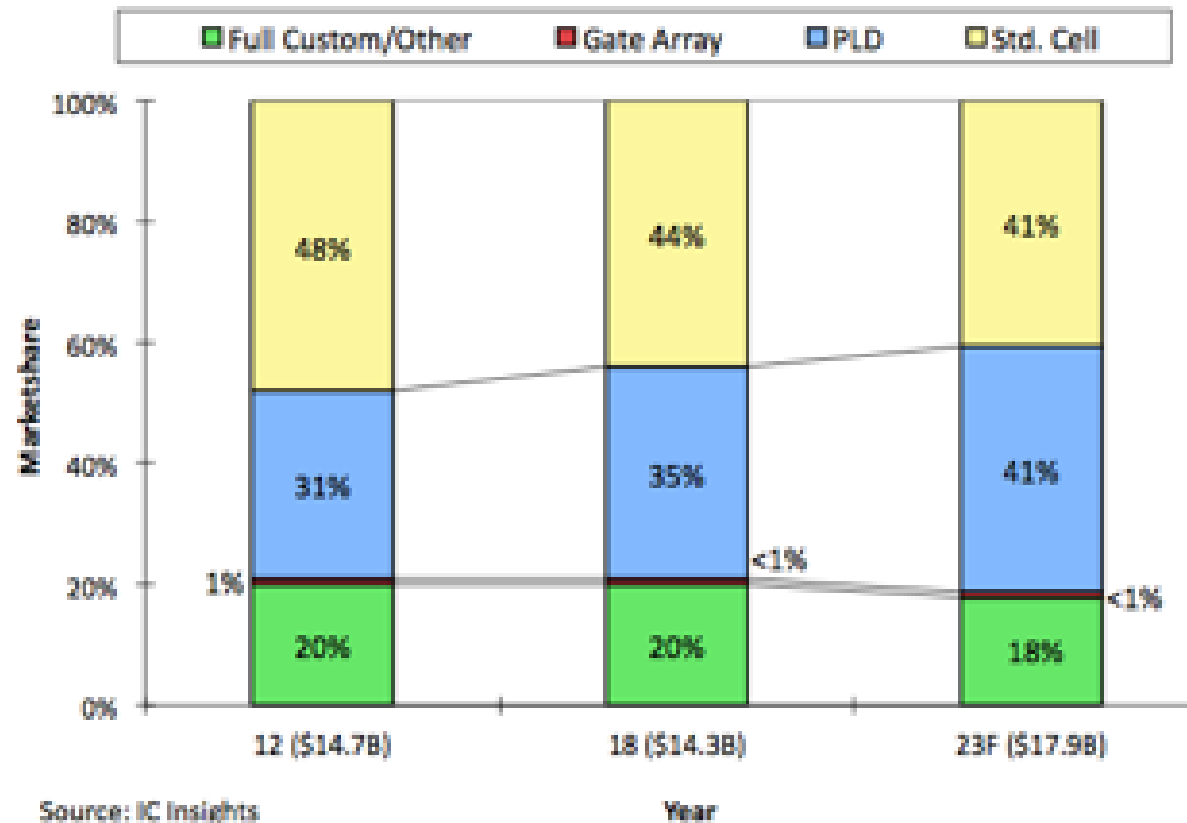
Embedded FPGA



# eFPGA



## ASIC Product Segment Marketshare



# Prelazno rešenje?



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## News Release

December 28, 2015

Share this Article



Contact Intel PR

## INTEL COMPLETES ACQUISITION OF ALTERA

SANTA CLARA, Calif., Dec. 28, 2015 – Intel Corporation (“Intel”) today announced that it has completed the acquisition of Altera Corporation (“Altera”), a leading provider of field-programmable gate array (FPGA) technology. The acquisition complements Intel’s leading-edge product portfolio and enables new classes of products in the high-growth data center and Internet of Things (IoT) market segments.



“Altera is now part of Intel, and together we will make the next generation of semiconductors not only better but able to do more,” said Brian Krzanich, Intel CEO. “We will apply Moore’s Law to grow today’s FPGA business, and we’ll invent new products that make amazing experiences of the future possible – experiences like autonomous driving and machine learning.”

Altera will operate as a new Intel business unit called the Programmable Solutions Group (PSG), led by Altera veteran Dan McNamara. Intel is committed to a smooth transition for Altera customers and will continue the support and future product development of Altera’s many products, including FPGA, ARM®-based SoC and power products. In addition to strengthening the existing FPGA business, PSG will work closely with Intel’s Data Center Group and IoT Group to deliver the next generation of highly customized, integrated products and solutions.

“As part of Intel, we will create market-leading programmable logic devices that deliver a wider range of capabilities than customers experience today,” said McNamara, corporate vice president and general manager of the Programmable Solutions Group at Intel. “Combining Altera’s industry-leading FPGA technology and customer support with Intel’s world-class semiconductor manufacturing capabilities will enable customers to create the next generation of electronic systems with unmatched performance and power efficiency.”

Intel expects the acquisition to be accretive to non-GAAP EPS and free cash flow in the first full year after close, consistent with prior guidance. Intel expects the acquisition to be dilutive to GAAP EPS in the first full year after close primarily due to acquisition-related costs.

ARM is a registered trademark of ARM Limited (or its subsidiaries) in the European Union and/or elsewhere. All rights reserved.

### Forward Looking Statements


This press release contains forward-looking statements, including statements concerning Altera’s development and sale of products and

[Home](#) > [Press Room](#)

# Xilinx FPGAs to be Deployed in New Amazon EC2 F1 Instances - Accelerating Genomics, Financial Analytics, Video Processing, Big Data, Security, and Machine Learning Inference

Amazon EC2 F1 instances to include latest Xilinx 16nm UltraScale+ FPGAs

Dec 7, 2016

 [Photos \(1\)](#)

SAN JOSE, Calif., Dec. 7, 2016 /PRNewswire/ -- Xilinx, Inc. (NASDAQ:XLNX) today announced that Amazon Web Services (AWS) is deploying Xilinx 16nm UltraScale+™ Field Programmable Gate Arrays (FPGAs) in the new Amazon Elastic Cloud Compute (Amazon EC2) F1 instance type, accelerating genomics, financial analytics, video processing, big data, security, and machine learning inference workloads.

In addition to Amazon EC2 F1 instances, AWS also announced an FPGA Developer Amazon Machine Image (AMI), which is pre-built with the development tools and scripts including Xilinx's Vivado® Design Suite and Vivado license.

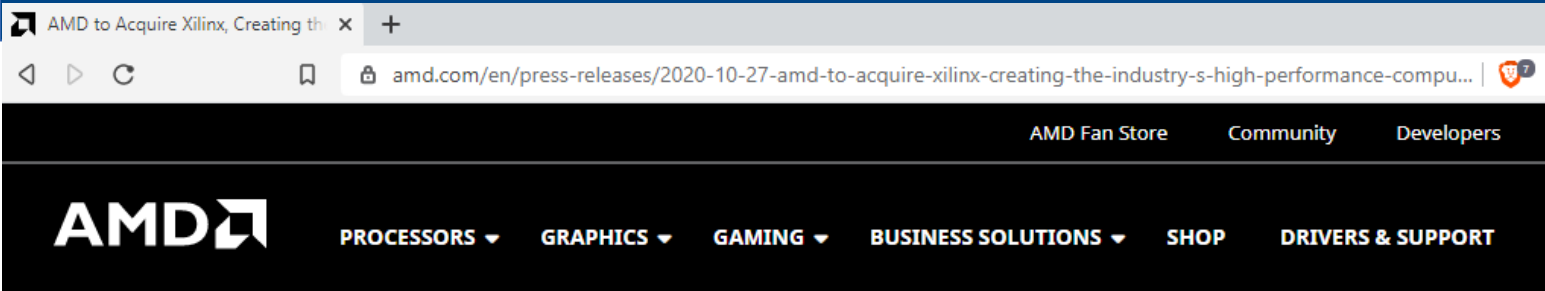
"We believe FPGAs are going mainstream in the cloud," said Steve Glaser, senior vice president, corporate strategy at Xilinx. "The AWS announcement last week is further evidence that this is happening right now and the momentum is building."

To learn more about the Amazon EC2 F1 instances web page at <https://aws.amazon.com/ec2/instance-types/f1/>, and AWS developer blog at <https://aws.amazon.com/blogs/aws/developer-preview-ec2-instances-f1-with-programmable-hardware/>.

## About Xilinx

Xilinx is the leading provider of All Programmable FPGAs, SoCs, MPSoCs, and 3D ICs. Xilinx uniquely enables applications that are both software defined and hardware optimized – powering industry advancements in Cloud Computing, 5G Wireless, Embedded Vision, and Industrial IoT. For more information, visit [www.xilinx.com](http://www.xilinx.com).





## AMD to Acquire Xilinx, Creating the Industry's High Performance Computing Leader

Share



— Strategic transaction strengthens AMD's industry-leading technology portfolio —

- Expands AMD's rapidly growing data center business
- Xilinx, the No. 1 provider of adaptive computing solutions, increases AMD TAM to \$110 billion
- Immediately accretive to AMD margins, cash flow and EPS
- All stock transaction with combined enterprise value of approximately \$135 billion

SILICON VALLEY, CALIF. 10/27/2020

AMD (NASDAQ: AMD) and Xilinx (NASDAQ: XLNX) today announced they have entered into a definitive agreement for AMD to acquire Xilinx in an all-stock transaction valued at \$35 billion. The combination will create the industry's leading high performance computing company, significantly expanding the breadth of AMD's product portfolio and customer set across diverse growth markets where Xilinx is an established leader. The transaction is expected to be immediately accretive to AMD margins, EPS and free cash flow generation and deliver industry-leading growth.

The acquisition brings together two industry leaders with complementary product portfolios and customers. AMD will offer the industry's strongest portfolio of high performance processor technologies, combining CPUs, GPUs, FPGAs, Adaptive SoCs and deep software expertise to enable leadership computing platforms for cloud, edge and end devices. Together, the combined company will capitalize on opportunities spanning some of the industry's most important growth segments from the data center to gaming, PCs, communications, automotive, industrial, aerospace and defense.

"Our acquisition of Xilinx marks the next leg in our journey to establish AMD as the industry's high performance computing leader and partner of choice for the largest and most important technology companies in the world," AMD President and CEO Dr. Lisa Su said. "This is truly a compelling combination that will create significant value for all stakeholders, including AMD and Xilinx shareholders who will benefit from the future growth and upside potential of the combined company. The Xilinx team is one of the strongest in the industry and we are thrilled to welcome them to the AMD family. By combining our world-class engineering teams and deep domain expertise, we will create an industry leader with the vision, talent and scale to define the future of high performance computing."

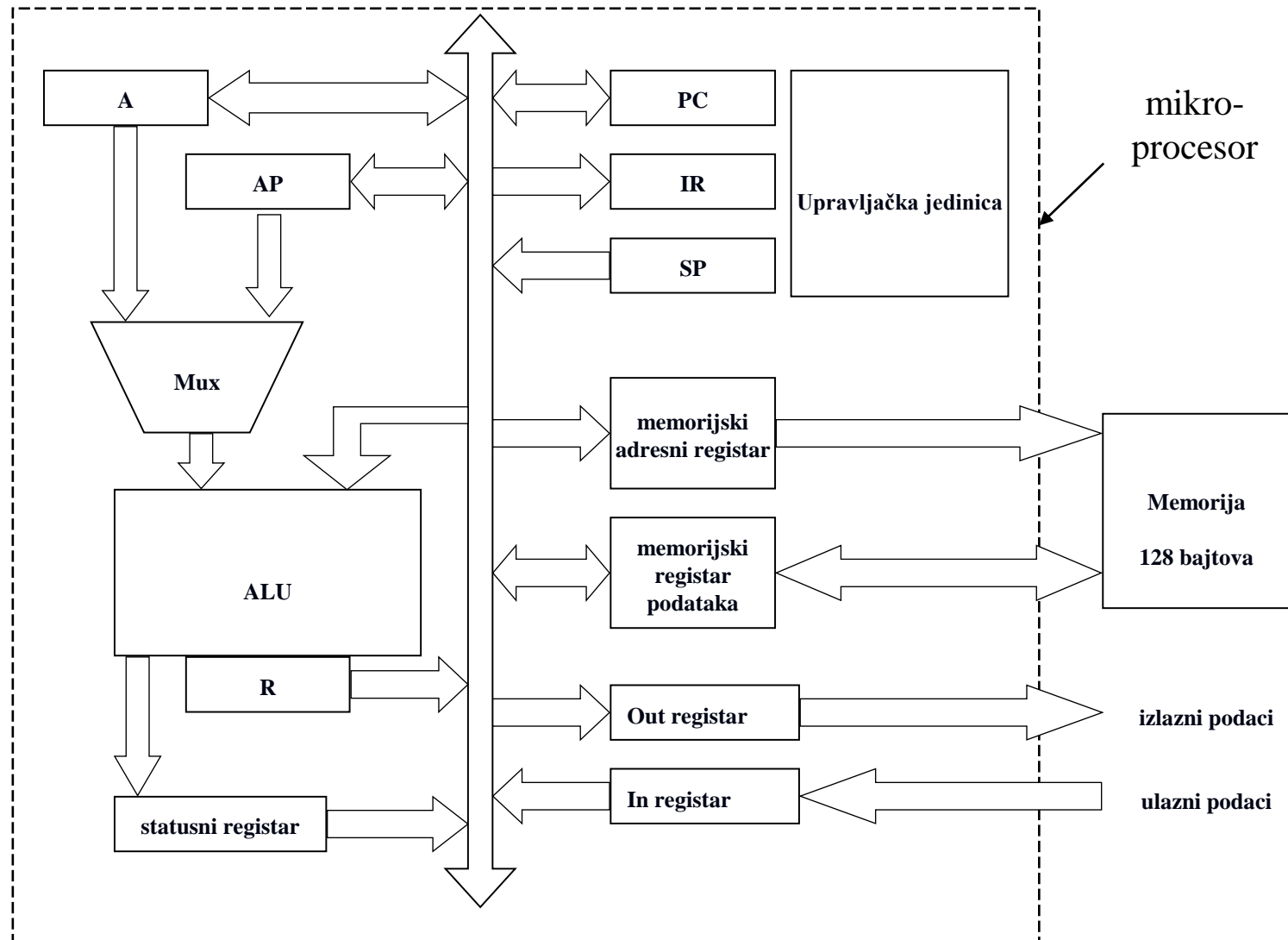
"We are excited to join the AMD family. Our shared cultures of innovation, excellence and collaboration make this an ideal combination. Together, we will lead the new era of high performance and adaptive computing," said Victor Peng, Xilinx president and CEO. "Our leading FPGAs, Adaptive SoCs, accelerator and SmartNIC solutions enable innovation from the cloud, to the edge and end devices. We empower our customers to deploy differentiated platforms to market faster, and with optimal efficiency and performance. Joining together with AMD will help accelerate growth in our data center business and enable us to pursue a broader customer base across more markets."

With a combined team of 13,000 talented engineers and over \$2.7 billion of annual<sup>1</sup> R&D investment, AMD will have additional talent and scale to deliver an even stronger set of products and domain-specific solutions.



# Edulent

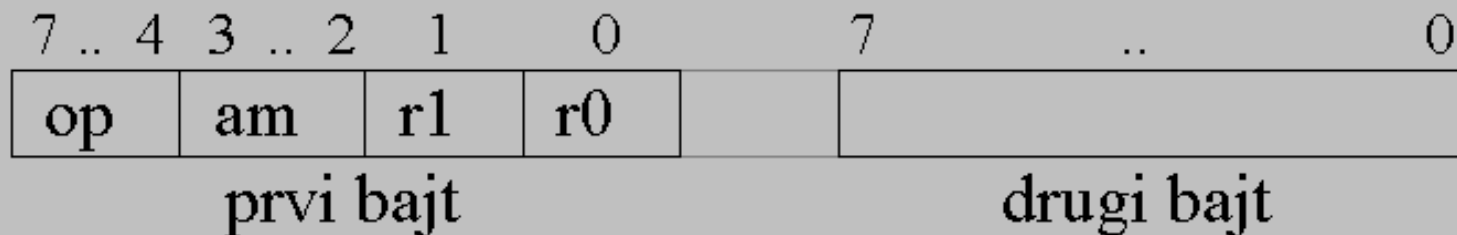
# Strukturalni model



**Tipovi adresiranja: direktno, neposredno, registarsko indirektno i predekrement / postinkrement.**

**Ukupno 39 instrukcija.**

**Format instrukcija:**



# Skup instrukcija

Dvobajtna instrukcija		Jednobajtna instrukcija	
		NOP	0x00
		END	0x02
MOV A, address	0x11	MOV A, [AP]	0x14
MOV AP, address	0x13	MOV A, [SP+]	0x1C
MOV A, const	0x19	MOV AP, [SP+]	0x1E
MOV AP, const	0x1B		
MOV address, A	0x21	MOV [-SP], A	0x2C
MOV address, AP	0x23	MOV [-SP], AP	0x2E
ADD A, address	0x31	ADD A, [AP]	0x34
ADD A, const	0x39		
ADD AP, const	0x3B		
SUB A, address	0x41	SUB A, [AP]	0x44
SUB A, const	0x49		
SUB AP, const	0x4B		
		NOT	0x50
OR address	0x61	OR [AP]	0x64
OR const	0x69		
AND address	0x71	AND [AP]	0x74
AND const	0x79		
XOR address	0x81	XOR [AP]	0x84
XOR const	0x89		
		SHR	0x90
JMP label	0xA1		
JZ label	0xA5		
JC label	0xA9		
CALL procedure	0xC1	RET	0xB0
		IN	0xD0
		OUT	0xE0

Mezei I. Evolution of an educational microprocessor.

Comput Appl Eng Educ. Wiley. 2020;1–13.

<https://doi.org/10.1002/cae.22300>

Core learning outcome	Edulent lectures	Edulent lab practice
CLO1	☑	☑
CLO2	Partially	☑ (ZEdulent)
CLO3	☑	
CLO4	☑	☑
CLO5	☑	
CLO6	☑	☑
CLO7	☑	☑
CLO8	☑	Partially
CLO9	☑	
CLO10		☑
CLO11		☑
CLO12	Partially	Partially

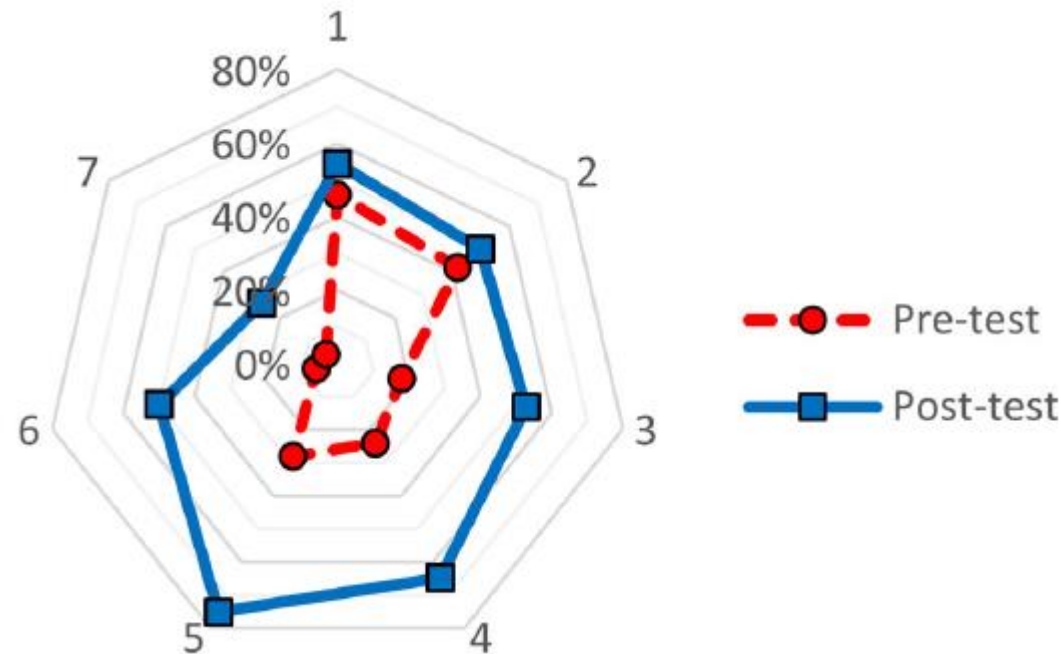
Using CE-CAO core knowledge units section in the IEEE/ACM curriculum guideline [11] we identified the following CLO:

1. Sketch a block diagram showing the main components of a simple computer.
2. Identify tools to simulate computer systems at different levels of design abstraction: system, instruction set processor (ISP), register transfer language (RTL), and gate level.
3. Explain the organization of a von Neumann machine and its major functional units.
4. Illustrate how a computer fetches from memory, decodes, and executes an instruction.
5. Articulate the strengths and weaknesses of the von Neumann architecture, compared to a Harvard or other architecture.
6. Describe the primary types of computer instructions, operands, and addressing modes.
7. Explain the relationship between the encoding of machine-level operations at the binary level and their representation in a symbolic assembly language.
8. Explain different instruction format options, such as the number of addresses per instruction and variable-length versus fixed-length formats.
9. Describe reduced (RISC) versus complex (complex instruction set computer [CISC]) instruction set computer architectures.
10. Write small assembly language programs to demonstrate an understanding of the machine-level operations.
11. Implement some fundamental high-level programming constructs at the assembly language level, including control flow structures such as subroutines and procedure calls.
12. Write small assembly language programs to access simple input/output devices using program-controlled and interrupt-driven methods.

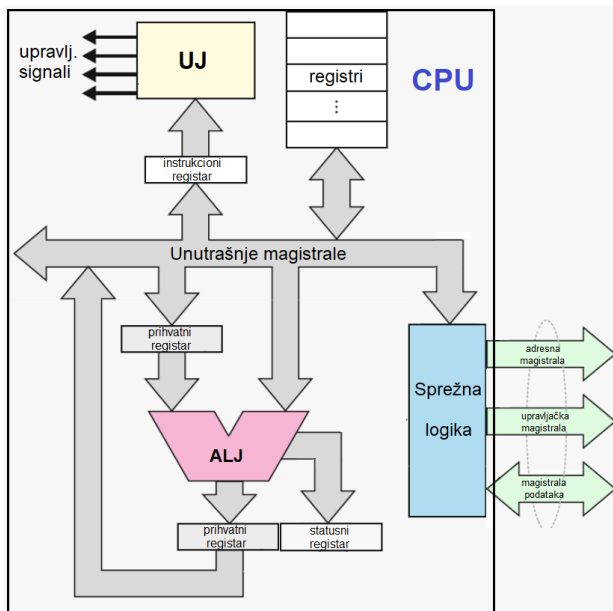
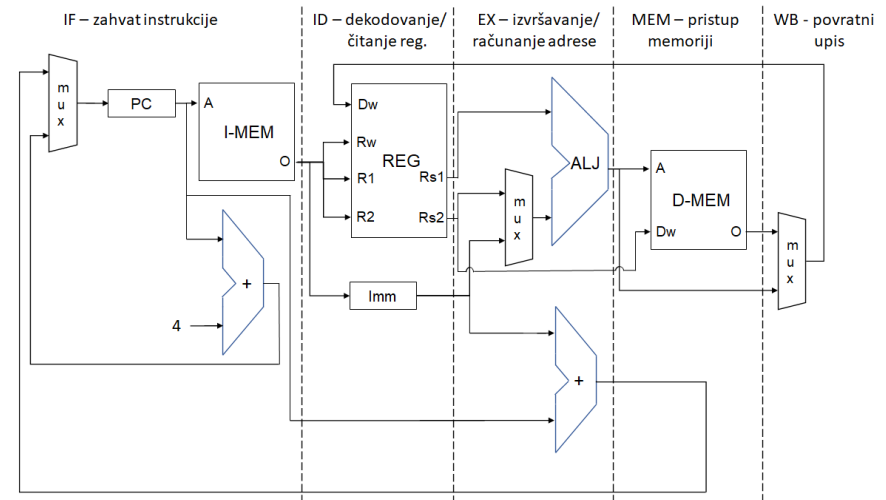
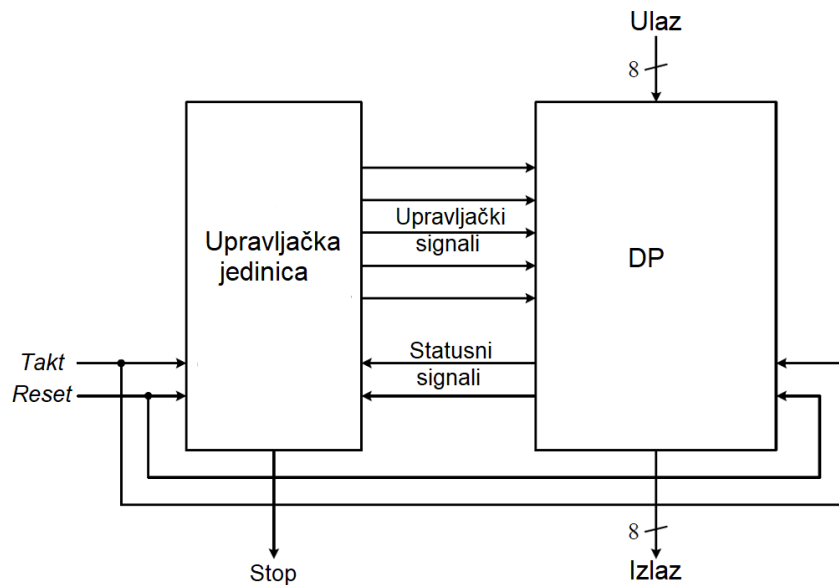
# Edukacioni značaj Edulenta

## Pretest and posttest questionnaire

#	Question	Level	Derived from
1.	<i>Explain the major functional units of the microprocessor.</i>	Basic	CLO3
2.	<i>What is the content of every program? Illustrate how programs are executed on the microprocessor.</i>	Basic	CLO4
3.	<i>Describe some types of instructions, operands, and addressing modes.</i>	Intermediate	CLO6
4.	<i>Explain the relationship between the encoding of machine-level operations at the binary level and their representation in a symbolic assembly language.</i>	Advanced	CLO7
5.	<i>What types of instruction format exist based on length size?</i>	Intermediate	CLO8
6.	<i>Explain the given fragment of 4 pseudo-instructions.</i>	Advanced	CLO10
7.	<i>What is the input/output mechanism of the microprocessor from the instruction point of view?</i>	Intermediate	CLO12



# Osnovi mikroprocesorskih i mikrokontrolerskih sistema



Hvala na pažnji!

