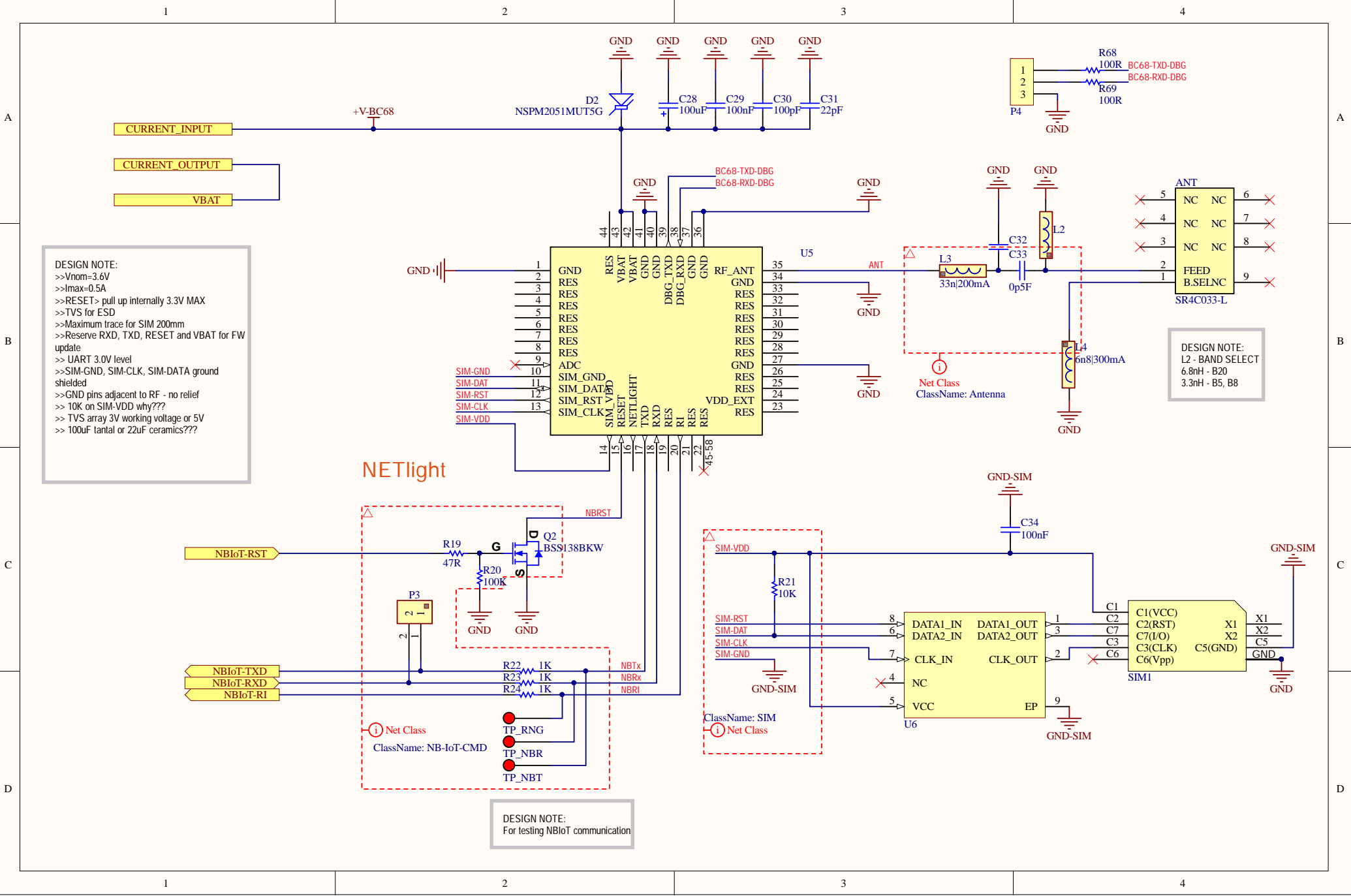


**Calculation of crystal load capacitors:**  
 $C_{ext} = 2 * (Crystal - C_{para} - C_{shunt})$

Crystal = 7.0pF (from crystal datasheet)  
 $C_{shunt} = 0.9pF$  (from crystal datasheet)  
 $C_{para} = C_{stray} + C_{pcb}$   
 $C_{stray} = (C_{in} * C_{out}) / (C_{in} + C_{out})$   
 $= (2.31 * 2.53) / (2.31 + 2.53)$   
 $= 1.2075pF$  (from device datasheet)  
 $C_{pcb} = 1pF$  (estimate)  
 $C_{para} = 1.21pF + 1pF = 2.21pF$   
 $C_{ext} = 2 * (7.0pF - 2.21pF - 0.9pF) = 7.8pF$

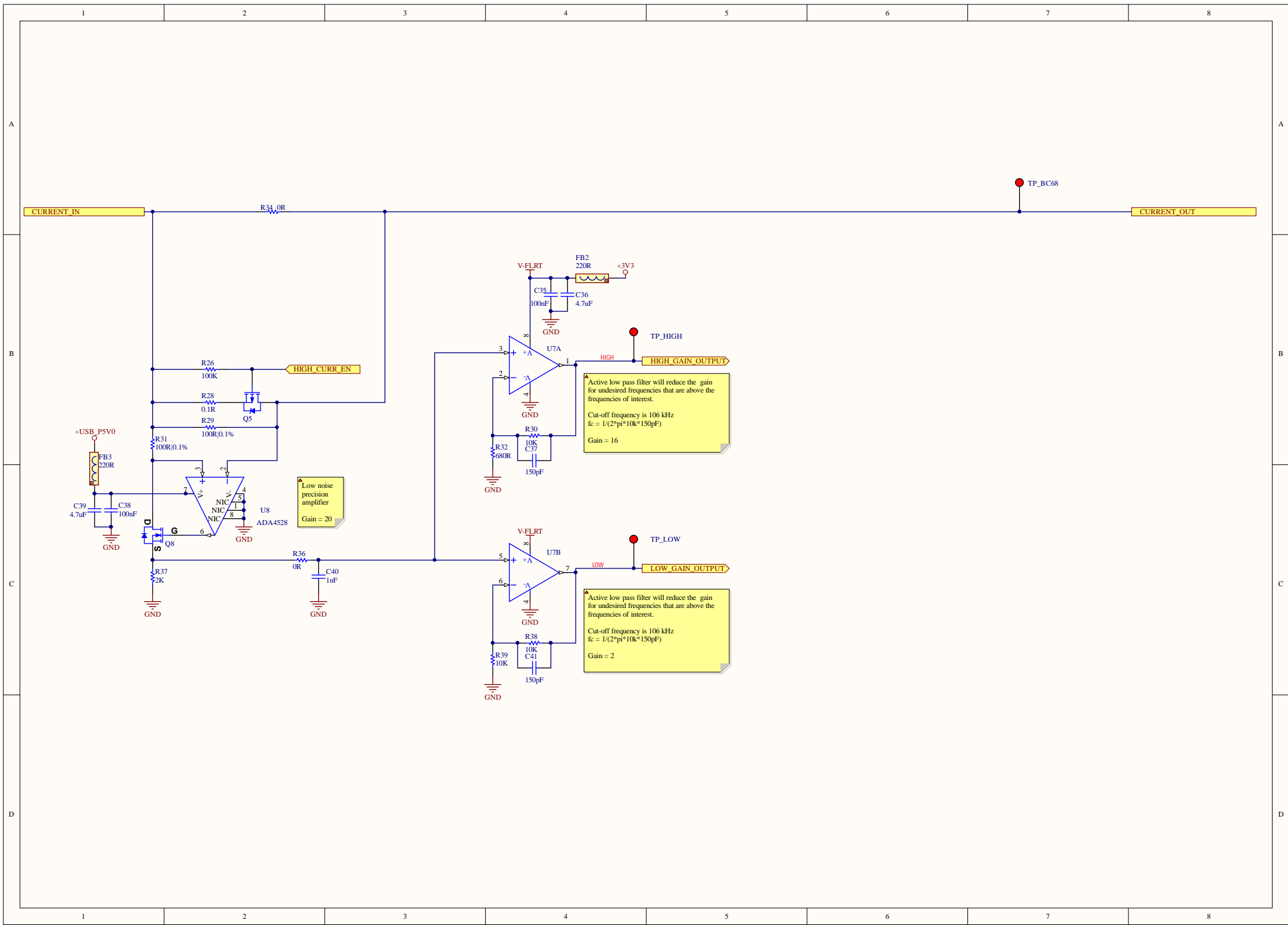
Selected in design: C=6.8pF  
 Verification show:  
 Accuracy (average on 9 DUTs): 11.6ppm  
 Startup time (first clock on output): 129ms  
 Safety factor: Above 10

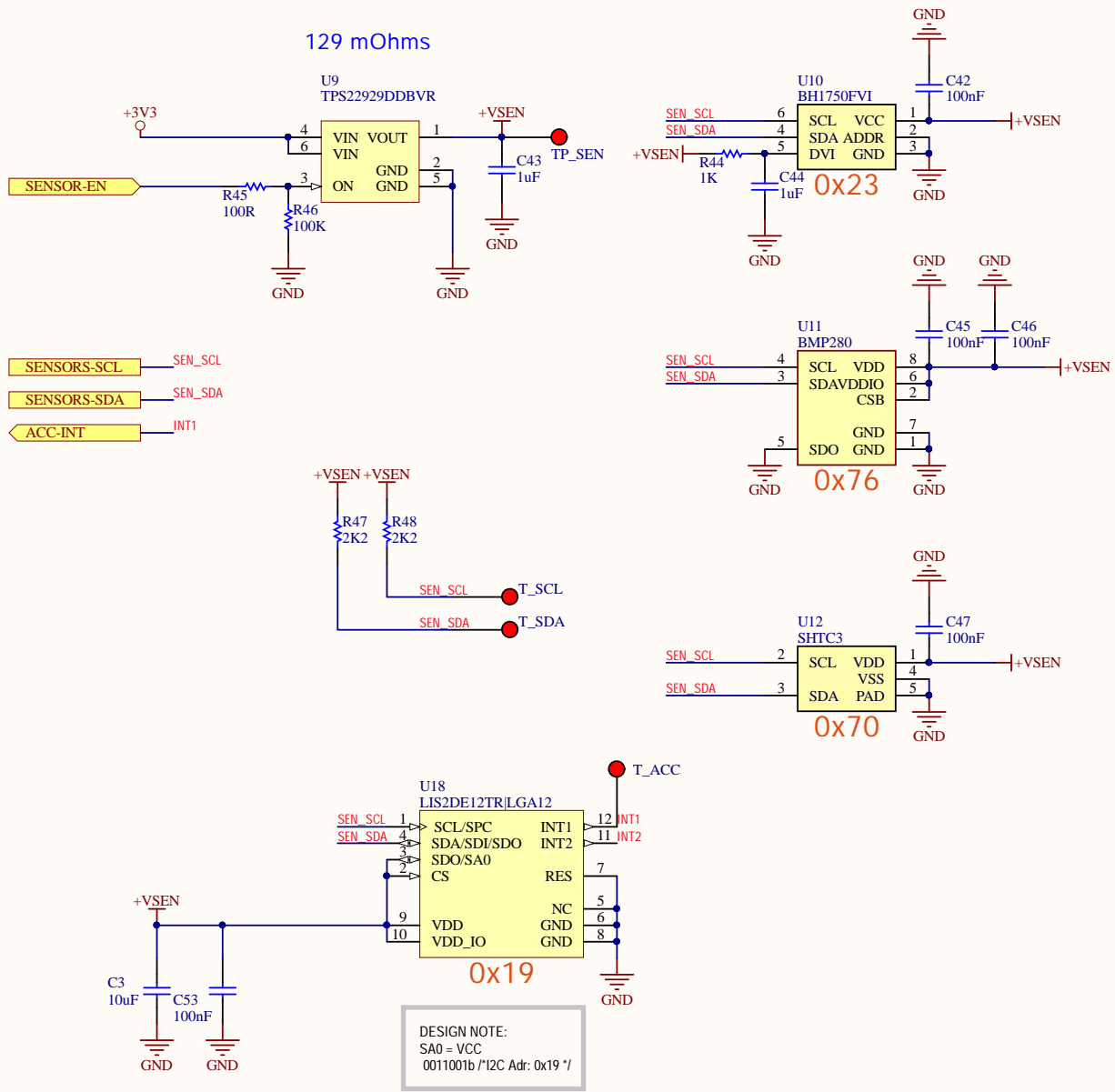


DESIGN NOTE:  
 >>Vnom=3.6V  
 >>Imax=0.5A  
 >>RESET> pull up internally 3.3V MAX  
 >>TVS for ESD  
 >>Maximum trace for SIM 200mm  
 >>Reserve RXD, TXD, RESET and VBAT for FW update  
 >> UART 3.0V level  
 >>SIM-GND, SIM-CLK, SIM-DATA ground shielded  
 >>GND pins adjacent to RF - no relief  
 >> 10K on SIM-VDD why???  
 >> TVS array 3V working voltage or 5V  
 >> 100uF tantal or 22uF ceramics???

DESIGN NOTE:  
 L2 - BAND SELECT  
 6.8nH - B20  
 3.3nH - B5, B8

DESIGN NOTE:  
 For testing NB-IoT communication





129 mOhms

0x23

0x76

0x70

0x19

DESIGN NOTE:  
 SA0 = VCC  
 0011001b /\*I2C Adr: 0x19 \*/

1

2

3

4

A

A

B

B

C

C

D

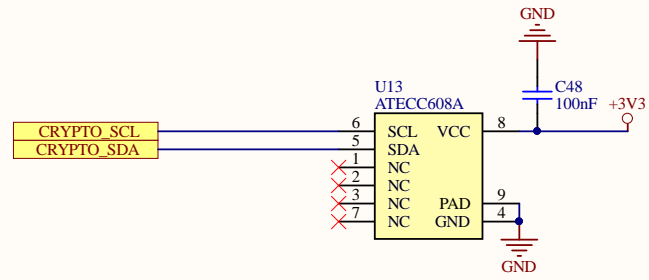
D

1

2

3

4



1

2

3

4

A

A

B

B

C

C

D

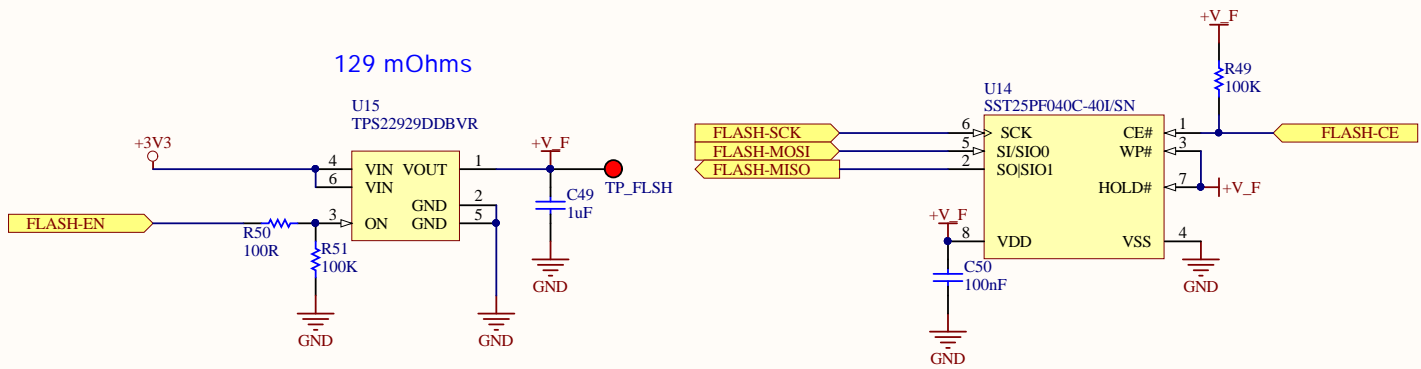
D

1

2

3

4



1

2

3

4

A

A

B

B

C

C

D

D

1

2

3

4

